RL-TR-91-155 Final Technical Report July 1991

## AD-A241 476



## COMPUTER AIDED ASSESSMENT OF RELIABILITY USING FINITE ELEMENT METHODS

**McDonnell Aircraft Company** 

D.A. Followell, S.L. Liguore, R. Perez, W.D. Yates III

SEP 3 0 1991,

APPROVED FOR PUBLIC RELEASE; DISTRIBUTION UNLIMITED.

91-11779

putes: All DIEC reproducttions will be in black and

Rome Laboratory
Air Force Systems Command
Griffiss Air Force Base, NY 13441-5700

91 9 27 1042

BEST AVAILABLE COPY This report has been reviewed by the Rome Laboratory Public Affairs Office (PA) and is releasable to the Mational Technical Information Service (NTIS). At NTIS it will be releasable to the general public, including foreign nations.

RL-TR-91-155 has been reviewed and is approved for publication.

APPROVED:

Pullen J. Brech WILLIAM J. BOCCHI

Project Engineer

APPROVED:

The "

A.

JOHN J. BART Technical Director

Electromagnetics & Reliability Directorate

If your address has changed or if you wish to be removed from the Rome Laboratory mailing list, or if the addressee is no longer employed by your organization, please notify RL(ERSD) Griffiss AFB NY 13441-5700. This will assist us in maintaining a current mailing list.

Do not return copies of this report unless contractual obligations or notices on a specific document require that it be returned.

# Public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, secretary general data needed, and computing and reviewing the collection of information, Send comments regarding this burden estimate or any core secretary collection of information, including suggestions for reducing this burden, to Washington Headquarters Services, Directorate for information Operations and Reports, 1215 Jefferson David Highway, Suite 1204, Arington, VA 22202-4302, and to the Office of Management and Budget, Paparvork Reduction Protect (0704-0188), Washington, Directorate (0704-0188), Washington, Dire

		The state of the s
1. AGENCY USE ONLY (Leave Blank)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	July 1991	Final Jun 89 - Dec 90
4. TITLE AND SUBTITLE		5. FUNDING NUMBERS
COMPUTER AIDED ASSESSME ELEMENT METHODS	NT OF RELIABILITY U	PE - 62702F
6. AUTHOR(S)		PR - 2338
D.A. Followell, S.L. Liguore, R	Perez, W.D. Yates III	TA - 02 WU - 3Y
7. PERFORMING ORGANIZATION NAME(S)	AND ADDRESS(ES)	8. PERFORMING ORGANIZATION
McDonnell Aircraft Company		REPORT NUMBER MDC B2303
P.O. Box 516		MBC 82303
St. Louis MO 63166-0516		
9. SPONSORING/MONITORING AGENCY N	AME(S) AND ADDRESS(ES)	10. SPONSORING/MONITORING AGENCY REPORT NUMBER
Rome Laboratory(ERSD)		DI TO OLISE
Griffiss AFB NY 13441-5700		RL-TR-91-155
11. SUPPLEMENTARY NOTES		
RL Project Engineer: William 3	Bocchi/RL(ERSD)/315	-330-4810.
12a. DISTRIBUTION/AVAILABILITY STATEME	NT	12b. DISTRIBUTION CODE

#### 13. ABSTRACT (Magriller) 200 words)

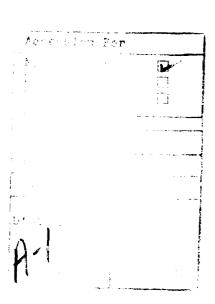
Approved for public release; distribution unlimited.

This report documents the development effort of a desk top reference handbook on how to use FEA results to predict electronic device life. The handbook is unique in several areas. Instead of being device oriented, it is oriented toward predicting material life for devices in certain system configurations and environments (i.e., instead of an LCC failure rate calculation, the solder joint fatigue life for an LCC device mounted to a circuit board subjected to a given RMS vibration load will be computed). The handbook contains the most comprehensive material data base available (under one cover) for FEA of electronic devices, and provides step-by-step examples (with number substitutions and units) for every failure mechanism and every material failure algorithm addressable by FEA. The procedures presented in this handbook can be applied to any electronics program to predict the life for electronic devices mounted in high stress areas. Familiarization with FEA procedures is assumed for the user of this handbook; however, guidelines are provided for applying FEA to microscale electronic structures.

14. SUBJECT TERMS Reliability, Finite Element	18 NUMBER OF PAGES 276		
Electronic Devices	- Marysis, Elle Frediction	<b>,</b>	16 PRICE CODE
17. SECURITY CLASSIFICATION UNCLASSIFIED	18. SECURITY CLASSIFICATION OF THIS PAGE UNCLASSIFIED	19. SECURITY CLASSIFICATION OF ABSTRACT UNCLASSIFIED	20. LIMITATION OF ABSTRACT SAR

#### **ACKNOWLEDGEMENT**

The authors wish to acknowledge the effort of Dave S. Steinberg of Steinberg and Associates for identifying many of the constraints for using finite element analysis for microscale electronic structures, for providing an insight into analytical methods of computing useable life of electronic components, and for providing material characterization data. The authors also wish to thank Bill Bocchi, the Program Manager at RL, and Marty Ferman, of McDonnell Aircraft Company (MCAIR), for their technical guidance. Finally, the authors wish to thank Debbie O'Hare, Barb Allen, and Dorothy Herbold of MCAIR for their word processing assistance; Rick Hermann of MCAIR for his administrative assistance: the Technical Graphics and Proposals Group of MCAIR for their graphics and page makeup support for this report; and Rick Nash of MCAIR for his excellent technical assistance in Finite Element Modeling.



#### TABLE OF CONTENTS

				Page
TAB	LE OF	F CONT	ENTS	iii
				vii
			S	viii
LIS	r of 1	rables		XV
EXE	ECUTI	VE SUM	IMARY	xvi
	pter 1 TE-Ol	F-THE-	ART ASSESSMENT	1-1
	1.0	Introd	uction	1-1
	1.1	Lite at	ure Search	1-2
	1.2	Univer	sities	1-4
		1.2.1	The University of Maryland	1-4
		1.2.2	The University of Wisconsin-Madison	1–4
	1.3	Indust	ry	1-5
		1.3.1	AT&T	1-5
		1.3.2	General Dynamics	1-6
		1.3.3	Westinghouse	1-8
		1.3.4	Martin Marietta	1-8
		1.3.5	Texas Instruments (TI)	1-9
		1.3.6	Hewlett-Packard (HP)	1-9
		1.3.7	Litton	1-9
		1.3.8	Pacific Numerix	1-9
		1.3.9	Engineering Mechanics Research Corporation (EMRC)	1-10
		1.3.10	Lockheed	1-12
		1.3.11	McDonnell Douglas Corporation	1-13
		1.3.12	Hughes Aircraft	1-14

				Page
1.4	4	U.S. Go	overnment Agencies	1-15
		1.4.1	National Institute of Standards and Technology	1–15
		1.4.2	Wright Laboratory (WL)	1–15
		1.4.3	Rome Laboratory (RL)	1-15
1.5	5	Finite I	Element Code Suppliers	1–16
Chapter	r 2			
ELECT	RO	NIC MA	TERIAL PROPERTIES	2–1
2.0	0	Introdu	action	2-1
2.	1	Failure	Mechanisms and Failure Modes	2-1
2.2	2	Genera	l Material Properties	2-4
2.3	3	Solder	Properties	2-8
2.4	4	Compo	nent Lead S-N Curves	2-20
Chapter	r 3			
FAILUI	RE N	иесна	NISMS	3–1
3.0	0	Introdu	action	3–1
3.	1	Deform	nation	3-1
3.2	2	Fatigue		3-2
3.3	3	Creep a	and Stress Relaxation	3-4
3.4	4	Fractur	e	3-6
		3.4.1	Ductile Fracture	3-6
		3.4.2	Brittle Fracture	3-8
3.3	5	Bucklin	ng	3-8
3 (	6	Failure	Modes of Electronics due to Failure Mechanisms	3_8

				Page
Chapter 4 FINITE E	LEMEN	T TECHN	HQUES	4–1
4.0				4-1
4.1			ods in Engineering Analysis	4-1
	4.1.1		lement Methods	4-2
	4.1.2		lement Computational Process	4-6
	4.1.3	General	Considerations and Guidelines	4–7
4.2	Source	es of Erroi	rs in a Finite Element Analysis	4-9
	4.2.1	Singular	ities	4-9
	4.2.2	Round-	off Errors	4-11
4.3	Finite	Element A	Accuracy in Stress Analyses	4-11
	4.3.1	Compat	ibility and Completeness of the Finite Element Mesh.	4-13
	4.3.2	Small E	lement Size Effects	4-14
	4.3.3	Beams of	of Two Materials	4-19
	4.3.4	Compar	ison of Linear and Nonlinear FEAs	4-20
4.4	Dynan	nic Model	ing/Analysis Technique for Electronic Equipment	4-26
	4.4.1	Determi	ning the Chassis to PCB Dynamic Coupling	4-27
4.5	Techni	ques for M	Modeling the PCB	4-30
4.6		_	wration Loads and Displacements onto Detailed Model of Component Leads	4-36
4.7	Model	ing Consi	deration for Leads and Solder Joints	4-47
	4.7.1	Plated T	Through Hold (PTH) Lead and Solder Joint Failures .	4-47
	4.7.2	Therma	Expansion Stress Analysis in DIPs	4-49
	4.7.3	Therma	Stress Analysis in LCCCs	4-52
4.8	Therm	al Stress !	Solder Joint Finite Element Analysis	4-56
	4.8.1	J-lead/S	solder Joint Finite Element Model Geometry	4-58
		4.8.1.1	ABAQUS & Nastran Finite Element Analysis of the J-lead/Solder	4-60
		4.8 1 2	J-Lead/Solder Joint Probe Finite Element Analysis	4-68

					Page
			4.8.1.3	J-lead/Solder Joint Probe FEA with Chip Carrier .	4–73
			4.8.1.4	J-lead/Solder Joint Probe FEA, Full 2-D Model	4-87
	•	4.8.2	Leadless	Solder Joint FEAs	4-97
			4.8.2.1	Leadless Solder Joint Probe FEA	4–97
			4.8.2.2	Leadless Solder Joint Probe FEA with Chip Carrier	4-105
			4.8.2.3	Leadless Solder Joint Probe FEA with Chip carrier and Thermal Loads	4-111
		4.8.3	Correlati	on of FEA Results and Known Failure Locations	4-121
Chapte					
RELIA	BILI	TY PRE	DICTION	NS	5-1
5.	.0	Introdu	ction		5-1
5.	.1	Deform	ation		5-1
5.	.2	Fatigue			5-1
		5.2.1	Finite El	ement Stresses for Fatigue Analysis	5-1
		5.2.2	Fatigue I	Life Prediction	5-6
		5.2.3	Fatigue I	Life Predictions Under Combined Stresses	5-7
			5.2.3.1	Independent Vibration and Thermal Stresses	5-8
			5.2.3.2	Generating Effective Strain vs. Life Curves	5-10
			5.2.3.3	Generating Effective Strain Histories	5-12
		5.2.4	Cyclic Pl	astic Stresses	5-16
5.	.3	Creep a	and Stress	Relaxation	5. 19
		5.3.1	Creep Fa	ailure Under Constant Load	5-19
		5.3.2	Combina	ation of Creep/Stress Relaxation and Fatigue	5-20
5.	.4	Fractur	e		5-23
		5.4.1	Brittle Fr	racture	5-23
		5.4.2	Ductile I	Fracture	5-24
5	٠.	Rucklin	ď		5 25

				Page
Chapter 6 RELIABIL	ITY AP	PLICATI(	ONS	6-1
6.0	Introd	uction		6-1
6.1	J-Leac	l Fatigue A	Analysis	6-1
	6.1.1	Thermal	Fatigue Analysis	6-1
		6.1.1.1	Lead Material Fatigue	6-3
		6.1.1.2	Solder Fatigue	6-3
	6 1.2	Vibratio	n Fatigue Analysis	6-4
		6.1.2.1	Lead Material Fatigue	6-5
		6.1.2.2	Solder Fatigue	6-8
6.2	LCC S	older Join	t Thermal Fatigue Analysis	6-9
	6.2.1	Thermal	Stress Analysis	6-9
	6.2.2	Fatigue	Life Prediction Based on Stress	6-12
	6.2.3	Fatigue	Life Predictions Based on Effective Strain	6-13
6.3	Dual-I	nline-Pac	kage (DIP) Lead/Solder Fatigue Analysis	6-15
6.4	Case S	tudy of M	MIC GaAs Component for Thermal Reliability	6-22
	6.4.1	Finite E	lement Analysis Results	6-24
	6 - 2	Gold Me	etalization Circuitry Reliability Prediction	6-33
		5.4.2.1	Linear Stresses and Neuber Rule Approximations .	6-33
		6.4.2.2	Thermal Cycles to Failure	6-36
	6.4.3	Gallium	Arsenide Reliability Prediction	6-39
6.5	Lead I	Buckling A	Analysis	6-39

#### LIST OF PAGES

Title Page	3-1 thru 3-10
i thru xx	4-1 thru 4-124
1-1 thru 1-22	5-1 thru 5-28
2-1 thru 2-24	6-1 thru 6-42

#### LIST OF FIGURES

	Title	Page
Figure 1-1.	State-of-the-Art Issues	1-1
Figure 1-2.	Circuit Board Used in ATA Analysis	1-7
Figure 1-3.	Finite Element Analysis of PCBs (FEAP)	1-11
Figure 1-4.	FEAP Life Prediction	1-12
Figure 1-5.	Gullwing Lead Finite Element Model	1-13
Figure 2-1.	"Black Box" Failure Modes & Mechanisms	2-2
Figure 2-2.	CTE for Common Materials	2-7
Figure 2–3.	Thermal Fatigue Data for LCC Solder Joints by I/O Count	2-10
Figure 2-4.	Strain Factor vs Cycles to Failure	2-10
Figure 2-5.	Stress vs. Strain for Solder	2-11
Figure 2-6.	Shear Stress-Strain Curve for Solder 63-37	2-11
Figure 2-7.	S-N Fatigue Curve for Soft Solder (50% Lead - 50% Tin), Reversed Bending	2-12
Figure 2-8.	S-N Fatigue Curve for Soft Solder (37% Lead - 63% Tin). Reversed Bending	2-13
Figure 2-9.	S-N Fatigue Curve for Soft Solder (50% Lead - 50% Tin). Reversed Shear	2-13
Figure 2–10.	S-N Fatigue Curve for Soft Solder (37% Lead - 63% Tin), Reversed Shear	2-14
Figure 2-11.	S-N Fatigue Curve for 67-37 Solder at Room Temperature	2-14
Figure 2-12.	Stress vs. Cycles to Failure	2-15
Figure 2-13	Thermal Fatigue Data for LCC Solder Joints	2-15
Figure 2-14.	Strain-Life Curve for 67-37 Solder at Room Temperature	2-16
Figure 2–15.	Strain Range-Fatigue Life Plots for 63/37 Sn/Pb Solder at Various Conditions	2-16
Figure 2-16	Solder Joint Stress Relaxation (63/37 Sn-Pb)	2-17
Figure 2-17	Solder Creep Properties	2-18

	litte	Page
Figure 2–18. Figure 2–19.	Strength vs. Strain Rate  Lifetime Data for Eutectic Solder Versus Percent Creep Per Cycle	2-18 2-19
figure 2-20.	Solder Modulus With Temperature	2-20
Figure 2-21.	Typical Random and Sinusoidal S-N Fatigue Curves for Kovar, Reverse Bending	2-21
Figure 2–22.	S-N Fatigue Curve for Electrical Lead Wire (99.9% Copper Cold Drawa). Reversed Bending	2-21
Figure 2-23.	S-N Fatigue Curve for Electrical Lead Wire (99.9% Nickel), Reversed Bending	2-22
Figure 2–24.	S-N Fatigue Curve for Electrical Lead Wire (99.9% Silver Hard Rolled), Reversed Bending	2-22
Figure 3–1.	Circuit Board Deformation During Temperature Cycles and Vibration	3-2
Figure 3-2.	Typical Format of Fatigue Data	3-3
Figure 3-3.	Fatigue Crack in a Leadless Solder Joint	3-3
Figure 3–4.	Fatigue Crack in a J-Lead Solder Joint	3-3
Figure 3-5.	Solder Creep and Stress Relaxation Behavior	3-4
Figure 3-6.	Solder Joint Stress Relaxation 63/37 Sn/Pb	3-5
Figure 3–7.	Hysteresis Curve for Materials Exhibiting Stress Relaxation	3-6
Figure 3-8.	Hysteresis Curve for Materials Which Exhibit Creep	3-6
Figure 3-9.	Stress Behavior in a Ductile Material as Applied Stress Increases	3-7
Figure 3–10.	Buckling Under a Compressive Load	3-8
Figure 4–1.	Uniform Bar	4-4
Figure 4-2.	Bar Math Model	4-4
Figure 4–3.	Finite Element Idealization	4-5
Figure 4-4.	Aspect Ratio for Quadrilateral Elements	4-12
Figure 4-5.	General Guidelines for Finite Element Modeling	4~13

	Title	Page
Figure 4-6.	Isotropic Panel With Circular Hole	4-14
Figure 4–7.	Isotropic Panel With Circular Hole - FEA Stresses	4–17
Figure 4–8.	Slender Beam With Two Materials and Square Cross-Section	4-19
Figure 4-9.	Tip Loaded Cantilever Beam With Two Materials - Mesh	4-19
Figure 4–10.	Stress and Strain Approximations	4-21
Figure 4–11.	Linear J-Lead FEA Analysis	4-23
Figure 4–12.	Stress - Strain Nonlinearity	4-25
Figure 4–13.	Printed Circuit Board Out-of-Plane Displacement	4-26
Figure 4–14.	Lead Displacement	4-27
Figure 4–15.	Electronic Chassis & PCB Assembly	4-28
Figure 4-16.	Chassis Assembly FEM	4-29
Figure 4–17.	Finite Elements for Structural Analysis	4-31
Figure 4–18.	Printed Circuit Board Boundary Conditions	4-32
Figure 4–19.	Half Model Finite Element Model Resonant Modes	4-33
Figure 4–20.	Full Finite Element Model Resonant Modes	4-34
Figure 4-21.	Small Lead Geometries	4-35
Figure 4-22.	Lead Grouping	4-35
Figure 4-23.	PCB Configuration	4-36
Figure 4-24.	Out-of-Plane Displacements	4–37
Figure 4–25.	Three Dimensional FEA Model	4-37
Figure 4–26.	J-Lead Axial Stiffness Representation	4-38
Figure 4–27	Relative Displacement - Chip to PCB	4-39
Figure 4-28.	Detailed Three-Dimensional J-Lead FEM	4-40
Figure 4-29.	Axial and Moment Displacement	4-40
Figure 4-30.	Load Transfer Analysis Results - Deformation	4-41

	litle	Page
Figure 4–31.	J-Lead Stresses	4-43
Figure 1–32.	Solder Stress	4-45
Figure 4–33.	Plated Thru Hole Z-Axis Expansion	4-47
Figure 4–34.	Plated Through Hole Section	4-48
Figure 4–35.	Three Dimensional Model Slice	4-49
Figure 4–36.	Quarter Model of DIP on PCB	4-50
Figure 4–37.	Thermal Expansion in Plane	4–51
Figure 4–38.	Modelling DIP Leads	4-51
Figure 4-39.	DIP Lead and Solder Model	4-52
Figure 4–40.	Highly Nonlinear Stress-Strain Curve	4-53
Figure 4-41.	Modulus Change With Temperature	4-53
Figure 4-42.	Strength vs. Strain Rate	4-54
Figure 4-43.	Constant Load vs. Life for Solder (Creep)	4-55
Figure 4-44.	Fatigue Life vs. Cycle Rate and Temperature	4–55
Figure 4-45.	Discretization Error Control	4-57
Figure 4–46.	J-Lead / Solder Joint Geometry	4-58
Figure 4-47.	ABAQUS FEM	4–59
Figure 4-48.	Loading and Imposed Displacements	4-61
Figure 4-49.	(a) Max Principal Stress - Nastran FEA	4-63
Figure 4-49.	(b) Max Shear Stress - Nastran FEA	4-65
Figure 4–50.	(a) Max Principal Stress - Probe FEA	4-69
Figure 4–50.	(b) Max Shear Stress - Probe FEA	4-71
Figure 4–51.	(a) Max Principal Stress - Probe w/Chip FEA	4-75
Figure 4–51.	(b) Max Shear Stress - Probe w/Chip FEA	4–77
Figure 4–51.	(c) Max Principal Stress – Probe w/Chip FEA	4-79

	litte	Page
Figure 4-51.	(d) Max Shear Stress - Probe w/Chip FEA	4-81
Figure 4-51.	(e) Max Principal Strain - Probe w/Chip FEA	4-83
Figure 4–51.	(f) Max Shear Strain - Probe w/Chip FEA	4-85
Figure 4–52.	(a) Max Principal Stress - Probe w/Thermal Loads	4-89
Figure 4–52.	(b) Max Shear Stress - Probe w/Thermal Loads	4-91
Figure 4-52.	(c) Max Principal Strain - Probe w/Thermal Loads	4-93
Figure 4–52.	(d) Max Shear Strain - Probe w/Thermal Loads	4-95
Figure 4–53.	Leadless Solder Joint Geometry	4-98
Figure 4-54.	Loading and Imposed Displacements	4-99
Figure 4-55.	(a) Max Principal Stress - Probe FEA	4-101
Figure 4–55.	(b) Max Shear Stress - Probe FEA	4-103
Figure 4–56.	(a) Max Principal Stress - Probe w/Chip FEA	4-107
Figure 4–56.	(b) Max Shear Stress - Probe w/Chip FEA	4-109
Figure 4–57.	(a) Max Principal Stress - Probe w/Thermal Loads	4-113
Figure 4–57.	(b) Max Shear Stress - Probe w/Thermal Loads	4-115
Figure 4–57.	(c) Max Principal Strain - Probe w/Thermal Loads	4-117
Figure 4–57.	(d) Max Shear Strain - Probe w/Thermal Loads	4-119
Figure 5-1.	Crack Propagation Controlled by Principal Stress	5-2
Figure 5–2.	Shear Deformation	5-3
Figure 5–3.	Miner's Rule Applied to Counted Effective Strain Ranges	5-7
Figure 5-4.	Slow Thermal Stresses and High Frequency Vibration Stresses	5-8
Figure 5–5.	Fatigue Data Obtained Under Fully Reversed Stresses	5-9
Figure 5-6.	Combined Manuever and Vibration Stresses	5-10
Figure 5-7.	Assembly of Effective Strain vs Life Curve	5-11
Figure 5-8.	The Strain Amplitude $\Delta\epsilon/2$ Can Be Obtained From the Stress-Strain Curve	5-12

	Title	Page
Figure 5-9.	Gaussian Distribution of Stress Amplitudes	5-12
Figure 5–10.	Rayleigh Distribution of Stress Peaks	5-13
Figure 5-11.	Model of Random Vibration With Blocks of Constant Amplitude Cycles	5-14
Figure 5–12.	Effective Strain Is Used to Predict Fatique Life	5-15
Figure 5–13.	Linear Elastic Cyclic Stress-Strain Behavior	5-16
Figure 5-14.	Plastic Stress-Strain Condition at the Peak of the Cycle	5-16
Figure 5-15.	Stress-Strain Behavior During a Reversed Load	5-17
Figure 5-16.	Hysteresis Stress-Strain Curves Under Fully Reversed Cycles	5-17
Figure 5–17.	Hysteresis Curve Generated From the Material Stress-Strain Curve	5-18
Figure 5–18.	Cyclic Stress-Strain Range	5-18
Figure 5-19.	Stress-Strain Loop During Constant Amplitude Cycles	5-19
Figure 5–20.	Creep Rupture Stress of Solder (60SN - 40 Pb)	5-20
Figure 5–21.	Relaxation of Thermal Stress in Solder	5-21
Figure 5–22.	Simplified Thermal Stress Model	5-22
Figure 5–23.	Combined Vibration Stresses and Thermal Stresses in Solder	5-22
Figure 5–24.	Solder Stress History Model	5-23
Figure 5-25.	Brittle Fracture	5-23
Figure 5-26.	Ductile Fracture	5-24
Figure 5-27.	Plastic Zone Surrounding a Crack Tip	5-25
Figure 5–28.	Out of Plane Board Deflections Can Cause Buckling of Leads	5-26
Figure 6-1.	J-Lead/Solder Joint Geometry	6-2
Figure 6–2.	Critical Areas Analyzed in the Thermal Cycle Reliability Assessment	6-2
Figure 6–3.	Constant Amplitude S-N Fatigue Curve for Electrical Lead Wire, Type D, Type K, Reversed Bending	6–3
Figure 6-4	Solder Stress-Strain Cycle in a I-Lead Connection	6-4

	Title	Page
Figure 6-5.	S-N Curve for 63-37 Solder at Room Temperature	6-4
Figure 6-6.	Critical Areas Analyzed in the Vibration Reliability Assessment.	6-5
Figure 6–7.	Random Amplitude S-N Fatigue Curve for Electrical Lead Wire, Type D, Type K, Reversed Bending	6-6
Figure 6-8.	Random Amplitude S N Fatigue Curve for Soft Solder (37% Lead - 63% Tin), Reversed Shear	6-8
Figure 6-9.	Constant Amplitude S-N Fatigue Curve for Soft Solder (37% Lead - 63% Tin), Reversed Shear	6-9
Figure 6–10.	2-D Model of a Leadless Chip Carrier and Solder Joint	6-10
Figure 6-11.	Shear Stress-Strain Curve for Solder 63-37	6-11
Figure 6–12.	Solder Stress-Strain Cycle in a Leadless Solder	6-12
Figure 6–13.	Strain-Life Curve for 63-37 Solder at Room Temperature	6-13
Figure 6–14.	Effective Strain vs Life for 63-37 Solder	6-14
Figure 6–15.	Thermal Expansion in Plane	6-16
Figure 6–16.	Typical DIP Package	6-18
Figure 6–17.	DIP Lead Deformation	6-19
Figure 6–18.	Transmit/Receive Module	6-23
Figure 6–19.	Driver Amplifier	6-23
Figure 6–20.	Temperatures in a 3 FET Cell Chip	6-25
Figure 6–21.	Thermal Model With Gold and GaAs Temperatures	6-27
Figure 6–22.	Principal Stresses in Gold Metallization	6-29
Figure 6-23.	Temperature vs Time for Two Pulses	6-31
Figure 6–24.	Stress-Strain Curve for Gold	6-34
Figure 6–25.	Gold Hysteresis Curve	6-35
Figure 6-26.	Stress History	6-37
Figure 6–27.	Fatigue Life From an Effective Strain vs Life Curve	6-38

#### LIST OF TABLES

	Title	Page
TABLE 1-1.	FINITE ELEMENT CODE SUPPLIERS	1–17
TABLE 1-2.	CODES AND METHODS MATRIX	1–17
TABLE 1-3.	FINITE ELEMENT APPLICATION	1-18
TABLE 2-1.	PREDOMINANT FAILURE MODES	2-3
TABLE 2-2.	MATERIAL APPLICATION AND FAILURE MODES	2-3
TABLE 2-3.	GENERAL MATERIAL PROPERTIES	2-5
TABLE 2-4.	GENERAL MATERIAL PROPERTIES - 2	2-6
TABLE 2-5.	CTE FOR ELECTRONIC MATERIALS	2–7
TABLE 2-6.	PCB LAMINATE PROPERTIES	2-8
TABLE 2-7.	SOLDER PROPERTIES	2-9
TABLE 3-1.	PREDOMINANT FAILURE MODES	3-9
TABLE 4-1.	FINITE ELEMENT SOLUTION ERRORS	4-9
TABLE 4–2.	INTERFACE STRESS DISCONTINUITIES	4-20
TABLE 4-3.	MATERIAL PROPERTIES	4-59
TABLE 4-4.	J-LEAD SOLDER JOINT STRESSES/STRAINS	4-67
TABLE 4-5.	THERMAL DISPLACEMENTS	4- 97
TABLE 4-6.	LEADLESS CHIP CARRIER SOLDER JOINT	4-100
TABLE 5-1.	APPLICATION OF FEA OUTPUT IN FATIGUE LIFE PREDICTION	5-5

#### **EXECUTIVE SUMMARY**

#### **Objective**

The objective of this study was to develop guidelines for using finite element analyses (FEA) to predict the life of new and untested electronic devices used in military equipment. Previously, there had been an inability to predict the life when empirically derived failure rates were not available. The techniques developed under this study are directly applicable to any advanced electronics acquisition. These procedures have been used on the Air Force Advanced Tactical Fighter (ATF) and the Navy Advanced Tactical Aircraft (ATA) programs to predict the life of critical electronic components.

Finite element analyses are computerized mechanical engineering techniques which make it possible to predict material response when a modeleu device is subjected to some internal or external loading or environmental disturbance. FEAs allow physical deflections, material stresses and material temperatures of complex devices to be predicted before the devices are fabricated and tested. Although this computer aided engineering (CAE) technique can successfully predict mechanical performance, a need exists to extrapolate FEA results to a prediction of life, time to failure or probability of failure. The latest developments in FEA technology relate to the interfacing of the results of FEA with reliability, or life prediction methodologies. Even though it is recognized that FEA simulations cannot address all possible failure mechanisms, improper fabrication procedures, etc., design evaluations and reliability assessments of electronics from a mechanical integrity and strength of materials perspective is achievable given the proper geometry, material, boundary conditions, loading, and strength information.

#### **Findings**

This study investigated and assessed the latest developments in FEA technology. It expanded the current mechanical/structural engineering FEA application techniques to electronic device and equipment applications, and resulted in a practical guide for electronic reliability assessment purposes.

Guidelines were developed to significantly improve the accuracy of finite element analyses of electronic devices. A method has been outlined which allows simplified linear FEAs to be used instead of the more complex elastic-plastic nonlinear FEA. Guidelines for mesh generation have been established which minimize arithmetic errors caused when materials with large stiffness differences are adjacent to each other. The accuracy of FEAs when dealing with very small dimensions has been verified. Procedures for combining various loadings in order to predict life have been established for materials which exhibit stress relaxation and for those which do not.

Existing computer codes were analyzed for applicability to electronic equipment along with their ease of use, versatility, and computational accuracy. The math models currently used to predict life were reviewed and documented. Materials used to manufacture electronic equipment and their respective failure mechanisms (which can be addressed by FEA) including buckling, deformation, rupture, fracture, property deterioration, fatigue, and creep were identified and documented. Additionally, the available physical properties of the materials which are necessary as inputs to FEA were collected and documented. A number of step-by-step examples were developed to illustrate how to predict the life of new untested electronic devices by utilizing FEA outputs.

Even though the procedures developed under this study can be directly applied to existing electronic programs, there are some limiting factors to institutionalizing the results of this study. These limiting factors are technology areas that require further development:

1) Validation of the prediction techniques: Life predictions using FEA outputs differ by as much as an order of magnitude from analytical techniques such as those of Steinberg and Engelmaier. None of the techniques have been verified by laboratory tests to confirm the accuracy of the life predictions. Each "expert" comes up with different answers to the same problem. Program managers are at a quandary because each "expert" believes their approach is the right one. However, none have been verified. This is probably the single most limiting factor.

- 2) Many material properties necessary for input to finite element codes are nonexistent. In many cases, properties for bulk materials are used. Materials sized at dimensions for electronic devices do not behave as materials sized at bulk level dimensions. Questionable input data translates to questionable analysis results.
- 3) Virtually every major electronic house and aircraft integrator are using some type of FEA procedures and reliability prediction tools. However, these are individual tools which require tedious, manual operations to finally arrive at a life prediction for electronic devices. Electronic design engineers require expedient, timely answers to their question regarding their designs. Fully automated computerized procedures are needed to perform electronic life predictions.

#### Study Approach

The study spanned 18 months and was subdivided into four tasks. A brief description of each task follows:

- 1) The first task was to determine the state-of-the-art of methodologies utilizing finite element output results for the prediction of reliability. This was accomplished through an extensive literature search, telephone interviews, and personal contact interviews at various meetings and symposia. The techniques utilized for predicting life of electronics by virtually every prominent electronics house, aircraft integrator, university, and government agency were identified and described. The algorithms and failure models of each methodology were identified. The reliability prediction techniques which use finite element analysis were reviewed and documented. The above was accomplished for commercially available codes which advertise or claim to be able to predict life or reliability, and for techniques used in industry which are not marketed as public domain commercial software.
- 2) The second task was to select a wide variety of materials which are used in electronic applications such as microelectronic and electronic devices, modules, circuit boards and packages. Failure mechanisms for the materials which could be addressed by finite element analysis were identified. The failure mechanisms were viewed from a perspective of material failures rather than device failures (ie., cracking of a material due to stress rather than fatigue failure of a specific device due to thermal cycling). Deformation, buckling, rupture or fracture, change or deterioration of material properties, fatigue and creep were among the failure mechanisms which were considered. Failure theories and material behavior models

- were evaluated and appropriate ones selected to predict life. The proper interfaces of the failure theories and material behavior models with the appropriate FEA results were identified. The prediction techniques selected were practical and useful for reliability assessments.
- 3) The third task was to develop a description of the above and present in a format which would allow easy application of the methodologies selected in Task 2 to electronic equipment. The result is the format of this final report.
- 4) The fourth task was to select examples and to demonstrate the application of making reliability assessments using FEA results coupled with material behavior models. Numerous examples were generated which show step-by-step procedures for predicting the life of electronic devices using FEA outputs. This task was accomplished by actually performing FEA using various finite element codes and comparing results. Known models were utilized to validate accuracy of small dimension modeling. Finally, examples were constructed which illustrate predicting life for materials exhibiting the various failure modes and mechanisms previously identified.

### Chapter 1 STATE-OF-THE-ART ASSESSMENT

#### 1.0 Introduction

This chapter describes the present state-of-the-art of methodologies utilizing finite element analysis (FEA) results for the prediction of reliability. The algorithms and failure models utilized by these methodologies are identified and described. Reliability prediction techniques that use finite element analysis are reviewed and documented. Commercially available codes that advertise or claim to be able to predict life or reliability are assessed, as are various techniques used in industry which are not marketed as public domain commercial software.

The assessment of the state-of-the art was accomplished by conducting an external and internal (to McDonnell Aircraft Company, hereinafter referred to as MCAIR) literature search and information survey (conducted over the telephone) to identify current finite element reliability analysis procedures (Figure 1-1). Information sources included universities, aerospace companies active in the design of electronics equipment, FEA code suppliers, various government agencies and McDonnell Douglas Corporation suppliers.

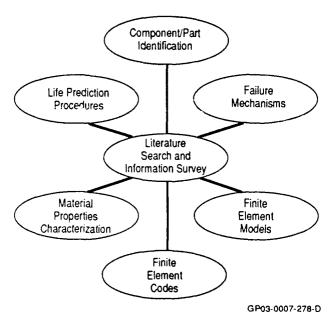


Figure 1-1. State-of-the-Art Issues

The conclusion reached is that there are various techniques to predict electronics reliability (life) utilizing FEA results. However, the following are technology areas that require further development:

- 1) Procedures have not been accurately validated by laboratory testing.
- 2) Most available packages use separate FEA procedures and life prediction tools.
- 3) There is no consensus as to the accuracy of, nor the exact techniques for, utilizing finite element modeling techniques for the extremely small scales required to analyze electronics components.
- 4) Material data required for analysis is ve / limited.

The following paragraphs describe the information obtained in researching the state-of-the-art of methodologies.

#### 1.1 Literature Search

In recent years, publications on the application of FEA to predict microelectronic reliability have been appearing at an explosive rate. This report will discuss some of the more pertinent works.

The study of finite element methods (FEM) to predict microelectronic reliability was initiated by Southland (Ref. 1–1). This study provided documentation and guidelines for the application of FEA to perform mechanical and thermal analysis of microelectronic packages. The study also included an assessment of various finite element codes and a set of guidelines to show how to apply FEA to electronic devices. The STARDYNE general purpose finite element code was determined to be the most applicable for analyzing electronic packages.

Computer aided engineering (CAE) software which predicts the vibration response of printed circuit boards (PCB) mounted within a line replaceable unit (LRU) was developed by Dandawante, Soovere and et al. (Ref. 1–2). This software was based on the finite element code entitled Numerically Integrated Elements for Structural Analysis (NISA). This report demonstrates finite element modeling and analysis techniques for

the prediction of stresses due to vibratory loads. NISA was previously identified by Southland et al. as having the capability of performing both vibration and thermal analysis. The advanced thermal analysis capabilities of NISA were demonstrated by Bivens and Bocchi (Ref. 1–3). Kallis et al. (Ref. 1–4) compared the capabilities of NISA to NASTRAN and ANSYS as a guideline to evaluate analyses that are done by government contractors using NASTRAN and ANSYS.

Soovere, Steinberg, Dandawate, and et al. (Ref. 1–5), developed a computer-aided design process to predict the dynamic stresses induced by vibration in leaded and leadless chip carriers (LCC) mounted on printed circuit boards. They demonstrated how these stresses (calculated using NISA) could be used to predict the fatigue life of electronic components.

Bivens and Bocchi used advanced finite element simulations to see how various physical factors affect surface mounted device temperatures. Detailed finite element modeling techniques for PCBs and LCCs were demonstrated.

Duncan et al. used finite element simulations to determine the stress levels in electronic packaging used in wafer scale integration (WSI). He then utilized the stress data to predict reliability.

The transfer of finite element output to a reliability assessment for solder connections was demonstrated by Bivens (Ref. 1-6). Solomon, Brzozowski and Thompson (Ref. 1-7), using 3-D FEA, showed how solder joint fatigue life could be predicted using joint strains and low cyclic fatigue data.

The earliest book which demonstrated an alternative approach to FEA for predicting mechanical reliability of microelectronic packages was given by Steinberg (Ref. 1–8). Steinberg developed a "cook book" approach for the shock and vibration analyses of electronic packages based upon empirical data and closed form solutions.

#### 1.2 Universities

Several universities are widely recognized for their research into the field of electronic life predictions and electronic material characterizations. The following two are the most significant.

#### 1.2.1 The University of Maryland

The University of Maryland has developed a program called Computer-Aided Life Cycle Engineering (CALCE) (Ref. 1-9). This software package performs automatic modeling based upon inputs by the user. CALCE provides the following modeling and prediction techniques:

- 1) Microelectronic package reliability modeling including wire and wire bond failure modeling, die attach failure modeling, corrosion failure modeling.
- 2) PCB packaging including the effect of components on PCB natural frequency, design techniques for fatigue of surface mount technology, coupled thermal and vibration fatigue analysis, and zonal decomposition techniques for thermal analysis. Currently, the vibration analysis is based on Steinberg's non-finite element methods. Finite element analysis tools for future versions of the software are being developed by the university. Fatigue life predictions are based on S-N data. PCB assembly packaging analysis includes forced convection cooling allocation and vibration analysis of edge conditions.
- 3) Interconnection and placement theory including placement for producibility.
- 4) Experimental measurement techniques including infrared experimental setup for PCB analysis and infrared studies on flaw detection.
- 5) Design matrix for system evaluation including introducing maintainability into the concurrent design process and a user definable derating system.
- 6) Lessons learned from MIL-HDBK-217 studies.

#### 1.2.2 The University of Wisconsin-Madison

The University of Wisconsin-Madison has an established Electronics Packaging and Interconnection Research Program (Ref. 1-10). The following three areas are the major thrusts of their program:

- 1) Isothermal fatigue testing of solder joint models Evaluation of material properties such as the modulus of elasticity, shear modulus and Poisson's ratio have been completed for bulk 60/40 solder. Current research employs shear specimens to develop life prediction methods for solder joints. The methods are based on calculations of damage from plastic strain and creep. In order to accurately account for damage, life vs. strain amplitude curves have been obtained for several temperatures.
- 2) SMT Package Test Methodology, Straddle Board Testing This area concentrates on measuring the stresses and strains that SMT packages experience during their lifetime. Straddle board tests permit fatigue life comparison between package designs. Real packages are tested in a controlled strain environment. Finite element modeling determines the stresses and strains that occur within the solder connections during loading.
- 3) Expert Systems The Expert Systems Software combines the stress and strain outputs from finite element modeling with the fatigue life data from the tests to determine the fatigue life of actual solder joints.

#### 1.3 Industry

The following paragraphs briefly describe the reliability (life) prediction activities by various members of industry which are involved in the design and analysis of electronic equipment.

#### 1.3.1 AT&T

Werner Engelmaier has developed many of the tools used by AT&T Bell Labs (Refs. 1–11,12,13). These tools are used to compute the thermal expansion mismatch between the board and the chip carrier based on the temperature distribution on the printed circuit board. This mismatch is computed with the following non–finite element relation:

$$\Delta \epsilon = \alpha_c (T_c - T_o) - \alpha_s (T_s - T_o)$$
 Eq. 1

where:  $\alpha_c$  is the coefficient of thermal expansion of the chip carrier

 $\alpha_s$  is the coefficient of thermal expansion of the substrate

T<sub>c</sub> is the maximum temperature of the chip carrier

T<sub>s</sub> is the substrate temperature

To is the initial temperature

 $\Delta \epsilon$  is the thermally induced expansion mismatch

AT&T then computes a shear strain from:

$$\Delta_{\gamma} = \frac{L}{\sqrt{2} h} \Delta \epsilon$$
 Eq. 2

where: L is the length of the chip carrier
h is the height of the solder joint

 $\Delta \gamma$  is the shear strain range

Their fatigue life computation uses the Manson-Coffin fatigue life relation to determine the cycles to failure based on the strain  $\Delta \gamma$ . Their analysis also includes models of the elastic-plastic and creep behavior of solder.

#### 1.3.2 General Dynamics

General Dynamics primarily uses Steinberg's non-FEA methods to predict the life of electronics (Ref. 1-14). In a recent study conducted for the US Air Force Advanced Tactical Aircraft (USAF-ATA), they applied these methods in the analysis of a circuit board containing surface mounted components (Figure 1-2). Two edges of the board are wedge clamped to the sides of the line replaceable unit (LRU), one edge is unrestrained and the board connection is on the other edge. They focused on a component with 68 gull-wing leads which had been located closest to the unrestrained edge of the board. Because of its location and size, this component will experience large vibration displacements and, therefore, large stresses in the leads.

GP03-0262-28

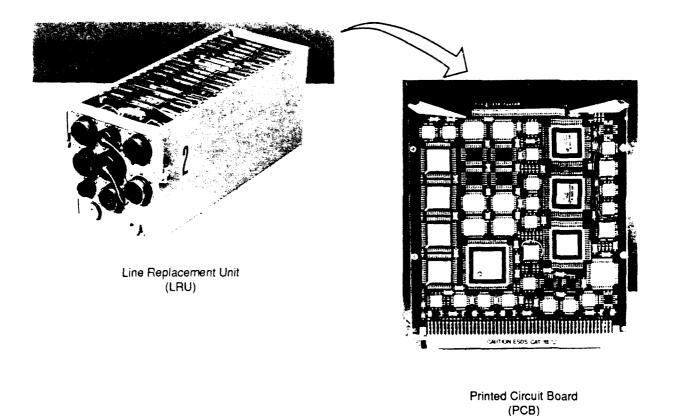


Figure 1-2. Circuit Board Used in ATA Analysis

The Steinberg based analysis resulted in a life prediction of 9,120 flight hours for the component. MCAIR completed a parallel effort as part of the same study, but used finite element methods to obtain the stresses in the lead and the solder joints of the same critical component. These stresses were then used in a Miner's cumulative damage analysis to predict the life of the component. MCAIR predicted a life of 117,905 flight hours. This comparison indicates that the Steinberg method results in a more conservative life prediction than does the finite element techniques. In addition to this work, general Dynamics has developed 3–D finite element models of leads and solder connections. They also have FEAP and the University of Maryland's CALCE software.

#### 1.3.3 Westinghouse

Westinghouse developed a FEA model for analyzing LCC solder joint stresses and strains induced by thermal or mechanical excursions under the Air Force contract F33615-82-C-5047, supported by the Wright Research and Development Center (WRDC) Materials Laboratory. The Westinghouse Electric Computer Analysis (WECAN) calculates the strain distribution in the solder joint for given loading conditions allowing the user to study the levels of strain and their location (Ref. 1-15). Westinghouse, a member of the CALCE consortium, is incorporating this software into its tools.

#### 1.3.4 Martin Marietta

The FEA code WECAN (developed by Westinghouse) was used by Martin Marietta to obtain Von Mises strain in solder joints (Ref. 1-7). Solder fatigue data was obtained in tests documented in Reference 1-16, work sponsored by the WRDC Materials Laboratory, Air Force contract F33615-85-C-5065. The shear strain  $\gamma$  was obtained from Von Mises strain  $\varepsilon_{vm}$  by:

$$\gamma = \sqrt{3} \epsilon_{\rm vm}$$
 Eq. 3

These strain computations were then used to predict the fatigue life of LCC solder joints. Martin Marietta has evaluated the effects of plasticity and crack propagation in the solder under the chip carrier and across the fillet.

Martin Marietta Electronic Systems in Orlando, FL is a subcontractor for the USAF-ATA. As part of this work, they predicted the life of several of the components in their designs (Ref. 1-17). Martin Marietta used coarse finite element models of circuit boards to determine vibration deflections and thermal deformations. This information was used as the boundary conditions for more detailed finite element models of the chip carriers mounted on the PCB. In the final step, detailed models of the solder joints yielded stresses used in a Miner's cumulative damage calculation to predict the creep/fatigue life of the components.

#### 1.3.5 Texas Instruments (TI)

The TI Materials and Control Group in Attleboro, MA, has used the ADINA finite element code to compute 3-D strains in chip mounts (Ref. 1-18). TI in Dallas has used ADINA to compute stress levels inside leaded chip carriers (chip, lead frame, chip pad, mold compound, and die attach) due to thermo-mechanical loads (Ref. 1-19).

#### 1.3.6 Hewlett-Packard (HP)

HP has completed FEA based thermal stress analyses of gullwing leads, their connection to the chip carrier and the solder joint connection to the board (Refs. 1–20,21). This work included evaluations of solder joint quality. HP has also completed FEA of J-leads, fatigue tests and statistical analyses of the test data. The tests involved boards loaded in cyclic four point bending until solder joint failures occurred.

#### 1.3.7 Litton

The current method used at Litton is Steinberg's non-FEA technique supplemented with finite element analyses of the board temperature distributions and board vibration. Although Litton is fully capable of generating detailed finite element models of leads and solder connections, their studies have shown that inaccuracies occur when using finite element analyses for stress and strain calculations in very small objects. FEA accuracy will be discussed in more detail later in the report. Because of the inaccuracies they found, Litton has concentrated on hand calculations to determine stresses in materials and predict their fatigue lives (Ref. 1–22). Thermal stresses are computed with strength of materials equations. Vibration analyses are based on resonant frequency equations modified with empirical factors. Fatigue life is then computed by adding the damage caused by vibration and by thermal cycles.

#### 1.3.8 Pacific Numerix

Pacific Numerix Corporation develops and markets specialized computer aided engineering software for the electronics industry. Pacific Numerix programs are used in the design and verification process to analyze the effects that parts, materials, component

placement and environmental conditions have on the performance, manufacturability, reliability, testability and maintainability of printed circuit boards.

Pacific Numerix programs comprise the PCB Design Expert System<sup>TM</sup> (PDES) and include (Refs. 1–23,24):

- 1) PCB Place Manual and automatic placement program
- 2) PCB Thermal Finite element printed circuit board thermal analyzer
- 3) PCB Vibration Finite element printed circuit board vibration analyzer
- 4) PCB Fatigue Finite Element Printed Circuit Board Stress/Fatigue Analysis Program

The board level thermal and vibrational results obtained from running PCB Thermal and PCB Vibration are automatically converted into appropriate boundary conditions and are applied to the detailed finite element models for stress analysis at the component level. PCB Fatigue performs thermal and vibrational FEA on critical detailed regions such as die bonds, bonding wires, solder posts, leads, plated thru holes and vias. PCB Fatigue also has the capability of analyzing the effects of parts tolerance and manufacturing process variability on the life of the equipment. The program automatically generates detailed finite element models for a variety of PCB assembly components.

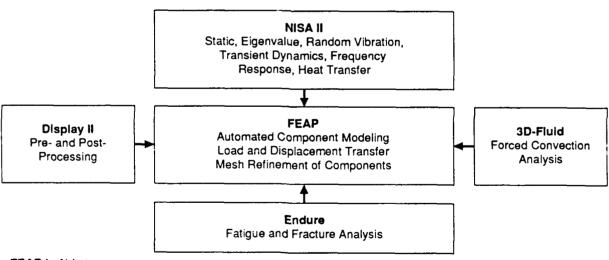
#### 1.3.9 Engineering Mechanics Research Corporation (EMRC)

EMRC has designed a program called Finite Element Analysis of PCBs (FEAP) which allows a structural engineer to model and evaluate PCBs and critical components without conducting expensive experiments. FEAP is able to predict temperature distributions across a PCB, calculate stresses in components, leads and PCBs due to vibration and thermal loads, and estimate the life of critical components.

FEAP (Figure 1-3) has a sophisticated built-in graphics capability which is geared towards helping the user define the PCB. Once the PCB and the components have been defined, FEAP generates a coarse finite element mesh for the entire board which includes modeling its critical components as plates and beams. After the finite element mesh of the

PCB and components is automatically generated, either heat transfer or dynamic analysis can be performed. Once the vibration or thermal analysis of the PCB has been completed. the forces, moments, displacements and rotations of the PCB are available at a preselected boundary on the PCB surrounding the electronic component selected for fatigue analysis. A much finer PCB mesh is then automatically generated for this component and a cubic interpolation is used to obtain a more detailed distribution of nodal forces and moments along the selected boundary. This unique sub-model approach improves the accuracy of the solution within a defined area of the PCB by applying the displacements/loads from the vibration or thermal analysis as statically imposed enforced displacements or loads. Further refinement can then be performed by generating a solid finite element model of the component and imposing the displacements/loads from the refined mesh analysis. Finally, built-in S-N fatigue curves are used to relate the FEA outputs (stress/strain) to component life (number of cycles to failure or lifetime) for common materials found in electronic assemblies. The fatigue life is predicted by searching the finite element model for regions of critical stress/strain and then using the appropriate cycles to failure curves (Figure 1-4) for the material with the high stress concentration.

FEAP Is Comprised of and Totally Integrates the Following Analysis:



FEAP is Able to:

- Predict Temperature Profiles
- · Calculate Stresses in Components, Leads, PCBs
- Estimate Life of Critical Components

2. Finite Florent Applicate of BODs (FF t.D)

GP03-0007-275-D

Figure 1-3. Finite Element Analysis of PCBs (FEAP)

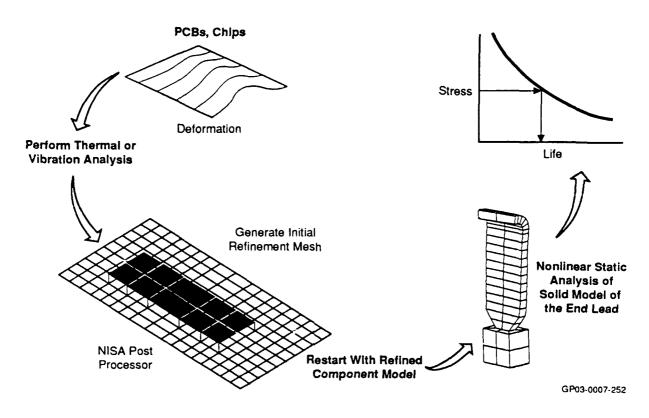


Figure 1-4. FEAP Life Prediction

#### 1.3.10 Lockheed

As part of a USAF – WRDC project (Contract Number F33615-85-C-3403), Lockheed has developed a finite element based reliability analysis in combination with EMRC and Steinberg and Associates (Ref. 1-5). The analysis uses the NISA finite element code with a pre-processor to model the geometries of the electronics and generate the finite element mesh. A post-processor displays the output stresses as contour plots which highlights the critical regions.

The output stress is then used to predict the cycles to failure by using stress versus life data for the given material. The life analysis model holds either vibration or thermal stresses constant while using the other to compute the life. Only linear material behavior is considered in the analysis. (Non-linear material behavior can occur if the yield strength of the material is exceeded and plastic deformation occurs.)

#### 1.3.11 McDonnell Douglas Corporation

MCAIR has applied FEA and fatigue life predictions to the Air Force version of the Advanced Tactical Aircraft (ATA) Flight Control Computer (Ref. 1–25). The fundamental frequency of the PCB and dynamic displacements were calculated with NASTRAN. The displacements were then imposed on detailed models of the leads and solder joints (Figure 1–5) to compute voration stresses. A similar analysis was completed to find the thermal stresses. The combined thermal-vibration stress history was then used in a Miner's Rule analysis to predict fatigue life. Solder joint geometry and solder quantity were varied to evaluate the impact of initial quality on stresses and life.

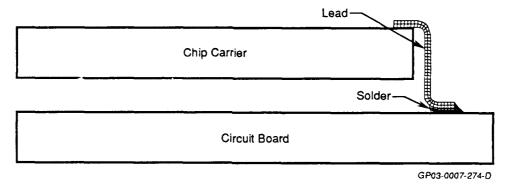


Figure 1-5. Gullwing Lead Finite Element Model

MCAIR is also developing simplified non-FE procedures to predict life based on stress computations using strength of materials equations. Miner's rule is used for life predictions. These procedures are being automated in the Fortran program "Electronics Life Prediction" (ELIFE). This code will serve as a quick analysis tool to isolate problem areas which may require subsequent detailed finite element analyses. The existing capability of ELIFE includes the following five analyses:

- 1) Thermal stress analyses of LCCs, leaded surface mount devices, dual-in-line packages (DIP) and plated through holes (PTH).
- 2) Thermal fatigue life computations for components in item (1).
- 3) PCB vibration analysis.
- 4) Vibration stress analysis of components in item (1).
- 5) Life predictions under combined thermal and vibration stresses.

Later versions of ELIFE will include a heat transfer analysis to calculate temperature distributions and an expanded component and material library.

McDonnell Douglas Electronics Systems Company, in combination with MCAIR, has tested printed circuit boards to obtain solder S-N fatigue data. These tests subjected surface mounted LCCs to thermal cycling.

#### 1.3.12 Hughes Aircraft

The Electro-Optical and Data Group within Hughes Aircraft is currently developing methods for analyzing cracks in avionics under the U.S. Air Force contract number F33615-87-C-3403 (Ref. 1-26,27). As part of this project, they evaluated failure sources in the Hughes APG-63 radar used in the F-15 aircraft. They have also fatigue tested wires in vibration, and thermally cycled wire bonds and plated through holes. Further tests will involve electronic assemblies subjected to thermal cycles.

Failure Analysis Associates has completed FEAs for Hughes to determine the stresses and strains in wire bonds exposed to mechanical loads. The calculated strains were similar to strains measured using stereoimaging methods developed at Southwest Research Institute. Southwest Research is also supporting Hughes with fracture mechanics analysis of cracks in electronics. The same group at Hughes has completed an FEA of wafer scale integrated devices as part of the USAF contract number F30602-87-C-0118 (Ref. 1-24). They compared NISA, ANSYS, and NASTRAN finite element codes and developed a computer program which uses finite element output stresses to compute fatigue life. This program contains a material properties database which covers low cycle fatigue (strain vs. cycles to failure), high cycle fatigue and crack growth data. The life computation does not account for mean stress effects which may occur when vibration and thermal stresses occur simultaneously or when the temperature cycle does not result in fully reversed strains.

#### 1.4 U.S. Government Agencies

#### 1.4.1 National Institute of Standards and Technology

The U.S. Department of Commerce National Institute of Standards and Technology sponsors electronic packaging workshops to establish material properties and measurement techniques (Ref. 1–28). Areas where their efforts are focused include test methods, mechanical properties and thermal properties. The materials of interest cover most electronic applications and include polymers, fiberglass, ceramics and metals. This type of data is essential for finite element based reliability assessments.

## 1.4.2 Wright Laboratory (WL) (Formally Wright Research and Development Center (WRDC))

The WL Environmental Control Branch compared finite element vibration analyses with tests and reported their findings in WRDC-TR-89-3110 entitled "Correlation/Validation of Finite Element Code Analyses for Vibration Assessment of Avionic Equipment" (Ref. 1-29). Plates, representing PCBs, were tested dynamically with various boundary conditions. Capacitors, diodes, transistors, relays and dips were mounted on the boards. The vibration frequencies of the boards were compared with calculated frequencies using NISA and NASTRAN finite element codes. The outputs of NISA and NASTRAN were within 5% of the measured vibration frequencies.

WRDC has also sponsored various contracted efforts in this area including the programs documented in References 1-2, 1-5, 1-7, 1-16, 1-26 and 1-27.

#### 1.4.3 Rome Laboratory (RL) (Formally Rome Air Development Center (RADC))

Extensive finite element analyses for electronics reliability assessments have been conducted at RL, Griffiss AFB, NY. (Refs. 1-3,6). Report RADC-TR-87-177, entitled "Reliability Analyses of a Surface Mounted Package Using Finite Element Simulation", documents efforts to analyze PCBs and electronic package assemblies to simulate the effects of die size, heat producing areas, voids in the die attach and thermal undercoat on the package thermal resistance using the NISA finite element code. The thermal

computations from the package/PCB analysis were then used in a 3-D finite element model of a leadless solder connection to compute thermally induced stresses for both models.

In another study (Ref. 1-6), 3-D NISA models were constructed of systems containing the chip carrier, circuit board and connections. The models included leadless, S-lead and gull-wing lead systems. Thermally induced deformations obtained with these models were then imposed on more detailed finite element models of the leads and solder connections. The output stresses were then used to estimate the strain amplitudes experienced during the thermal cycles. Life predictions were then obtained from material curves of strain versus cycles to failure.

RADC also sponsored projects documented in report RADC-TR-82-133, entitled "Finite Element Analysis of Microelectronic Packages" (Ref. 1-1) and efforts by Hughes Aircraft under contract number F30602-87-C-0018, entitled "Reliability Assessment of Wafer Scale Integration Using Finite Element Analysis" (Ref. 1-4).

## 1.5 Finite Element Code Suppliers

Table 1-1 lists the suppliers, the name of the finite element code and the purpose of the code for state-of-the-art finite element codes presently used within industry for reliability (life) analysis. All of these can be used to predict stress and strain levels in electronic components; however, the ability to do automated packaging analysis from a reliability standpoint is limited to the Pacific Numerix and EMRC codes. FEAP automates and integrates the capability to do stress analysis and life prediction into one package.

The matrix shown in Table 1-2 summarizes the applicability of various finite element and non-finite element techniques to fundamental electronic reliability analyses. Additionally, Table 1-3 identifies the unique characteristics of the FEA codes as they apply to structural mechanics applications, heat transfer applications and to fatigue and fracture mechanics applications.

TABLE 1-1. FINITE ELEMENT CODE SUPPLIERS

Code	Supplier	Purpose
ABAQUS	Hibbit, Karlsson, and Sorensen Inc.	Commercial/General
ADINA	ADINA R&D Inc.	Commercial/General
ANSYS	Swanson Inc.	Commercial/General
IDEAS	Structural Dynamics Research Corp.	Commercial/General
MSC/NASTRAN	MacNeal-Schwendler Corp.	Commercial/General
FEAP/NISA II	Engineering Mechanics Research Corp.	Commercial/General
PDES	Pacific Numerix Corp.	Commercial/Electronic Packaging
PROBE	MacNeal-Schwendler Corp. (formally of Noetic Technologies)	Commercial/Stress Analysis
WECAN	Westinghouse R&D Center	Commercial/Electronic Component Analysis

GP03-0007-273-D

TABLE 1-2. CODES AND METHODS MATRIX

		omplex he Ana		Rep	Representing the Failure Mechanism			nput Da Iracteri				nputati acy Eff		у	Applications			
	Finte Element Based	Strength of Material	Specific to Electronic Application	Deformation	Buckling	Rupture	Fatigue	Сгеер	Interactive	Automated Finite Element	Finite Element Batch	Very Accurate	Average Accuracy	Very Efficient	Average Efficiency	Much Involved Effort	Total Life	Crack Growth
ABAQUS	X			Х	Х	Х	Х	Х			х	Х				х		
ADINA	Х		<u> </u>	X	х	х	×	х			х	х				x	1	
AER	.,.,,.,		X		<b>.</b>	<b></b>			Х					Х	İ		Х	
ANSYS	Х			Х	X	Х	Ϋ́	Ÿ			Х	Х				Х		
ASME			[ [		ĺ	[			Х			ĺ	Х	X.			×	
CILIFE									X				Х	X	<b>.</b>		X	
CGLIFE									Х		1		X	X	1			X
Cracks 84					l				Х			ŀ	Х	Х	l			X
Beiger		X							X				X	X	ļ	<b></b>	ΧΧ	
IDEAS	Х			X							X		X			Х		
MTS									Х				Х	Х			Х	
MIT									X				X	X	ļ			X
NASGRO	, l			.,	١.,	.,			Х				X	X				X
NASTRAN NISA/FEAP	X			X	X	X	X	X			X	X			x	X	J.	
Pacific Numerix			X	X			X	X		X	X	X			ĝ		X	×
Probe	x		^	x						^	X	X			l ^	x	Х	
SAE	^			^					x		^	^	x	x	l	^	x	
Steinberg		X		x	X		X		l	·			^	·····^	ļ		^	ļ
Wecan	х	<u> </u>		x	^	x	^	x	^		x	х	^		i	×	^ :	
Risk				``		``		^	x		^	^	х	x		^		x

GP03-0624-71-D

TABLE 1-3. FINITE ELEMENT APPLICATION

	197	Sand		MAD.	MAGE	W.S.	1 / S	PR086
Structural	Mech	anics	Appli					$\mathcal{A}$
Types of Elements - 3-D Rod - 3-D Beam - Plane Stress - Plane Strain - Wembrane - Shear Panels - Plates - Thin Shells - 3-D Solids - Discrete Stiffness - Boundary - Gap	X X X X X X X X X X X X X X X X X X X	X X X X X X X X X X X X X X X X X X X	X	X X X X X X X X X X X X X X X X X X X	X	X X X X X X	x x x	X X X X
Range of Applications  Unear Statics  Eigenvalue  Free Vibration  Bucking  Nonlinear Statics  Response  Postbuckling  Nonlinear Dynamics  Nonlinear Upramics  Nonlinear Vibration  Transient  Nonlinear Interaction  Fluid-Structural  Thermal-Mechanical  Idiaticity  Static  Dynamic	X X X X X X X X	X X X X X X X	x x x x x x	X X X X X X X	X X X X X X	x x x x	x x	×××
Solution Techniques  Nonlinear Statics Incremental Newton-Type Nonlinear Dynamics Model Superposition Direct Integration Explicit	X X X	x x x	X	X X X	X X	x x		
Types of Loading  Concentrated  Line Thermal Random Deformation Dependent Initial Stress	X X X	X X X	X X X X	X X X	X X X X	X X X	X X X	X X X
Support Conditions  • Prescribed Displacement • Clastic Foundation	X X	X X	X X	χ	X	X X		X X
Material Properties  • sotropic  • Anisotropic  • Multilayered  • Temperature Dependent  • Elastic-Strain Hardening  • Viscoelastic  • Nominear Elastic  • Viscoplastic  • High Temperature Creep	X X X X X X X X X X X X X X X X X X X	X X X X X X X	X	X X X X X X X X X X X X X X X X X X X	X	× × × × × × × × ×	X X	X X X

	Jan Jan	Salas	T ANGE	MADO	MAG	W.S.	1 / 2	PRO6 14
Heat Tr	ansie.	Appi	icatio		<u> </u>		/	
Space Dimensionality  • 3-0  • 2-0	X X	X	x	X	X	X	×	х
Range of Applications  • Linear Steady State  • Nonlinear Steady State  • Linear Transient  • Nonlinear Transient	X X X	X X X	X X X	X X X	X X X	X X X	x	x
Material Properties  • isotropic  • Anisotropic  • Multiayered  • Temperature Dependent  • Time Dependent	X X X X	X X X X	X X X	X X X X	X X	X X X	x	×
Boundary Conditions  • Prescribed Temperature  • Convection From a Surface  • Radiation	X X X	X X	X X	X X	X X	X X	X X	X
Other Capabilities • Thermal-Stress Coupling	х	x	x	х		х		X
Faligue and Frac	ture f	Mecha	nics .	Applic	ation	ıs		
Types of Elements Plane Stress Plane Strain Plates Thin shells Thick Shells 3-D Solids	X X X X X	X X X X	X X	X X X X	X X X X	X X X X X		XXXX
Range of Applications  • Linear Statics  • Nonlinear Statics  • Nonlinear Dynamics	×	X X	X X X	X X	X X X	X X		x
Loading Static Function of Time Mode I Mode II Combines Modes Initial Stress	X X X X X	X X X X X	X X X	X X X X X X	x x x x x	X X X X X		X X X X
Surface Crack Geometry • Straight • Curve	×	X	x	X X	X X	×		X X

GP03 0624-72-0

#### References

- [1-1] Southland, J.R. Beatty, V.R., and Vitaliano, W.J., "Finite Element Analysis of Microelectronic Packages," RADC-TR-82-133, May 1982.
- [1-2] Soovere, J., Dandawate, B.V.; "Vibration Stress Analysis of Avionics", AFWAL-TR-87-3023; April 1987.
- [1–3] Bivens, G.A., and Bocchi, W.J., "Reliability Analyses of a Surface Mounted Package Using Finite Element Simulation," RADC-TR-87-177, October 1987.
- [1–4] Kallis, J.M., Duncan, L.B., Van Westerhuyzen, D.H., Sandkulla, D.C., MacFarlane, J.D., Naepflin, H.P., Ingersoll, J.G., Tierney, B.D., McHorney, P.E., Erickson, J.J., and Terrill, K.W., "Reliability Assessment of Wafer Scale Integration Using Finite Element Analysis", Hughes Aircraft Company under RADC contract number F30602–87–C–0118, February 1990.
- [1-5] Soovere, J., Dandawate, B.V., Garfinkel, G.A., Isikbay, N., and Steinberg, D.S., "Vibration Reliability Life Model for Avionics," AFWAL-TR-87-3048.
- [1-6] Bivens, G.A., "Reliability Assessment Using Finite Element Technique," RADC-TR-89-281, Nov 1989.
- [1-7] H.D. Solomon, V. Brzozowski, and D.C. Thompson, "Prediction of Solder Joint Fatigue Life," AFWAL-TR-89-4002, April 1988.
- [1-8] Steinberg, D.S., "Vibration Analysis for Electronic Equipment," John Wiley and Sons, 1973.
- [1-9] Conversation with Michael Pecht, Director of CALCE, University of Maryland, 1989.
- [1-10] Conversation with Bela Sandor, Director of the Electronics Packaging and Interconnection Program, University of Wisconsin-Madison, 1989.

- [1-11] Engelmaier, W., "Reliability of Surface Mounted Assemblies: Controlling the Thermal Expansion Mismatch Problem," Presented at the SMART IV Conference, Los Angeles, CA, January 11-14, 1988.
- [1–12] Engelmaier, W., "Fatigue Life of Leadless Chip Carrier Solder Joints During Power Cycling," Proceedings of the Technical Program of the 2nd Annual International Electronics Packaging Society Conference, San Diego, CA, November 15–17, 1982.
- [1-13] Engelmaier, W., "A Reliability Test," Circuits Manufacturing, June 1988.
- [1-14] Conversation with Jeff Intrieri, General Dynamics Fort Worth Division, 1989.
- [1-15] WECAN Westinghouse Electric Computer Analysis, User's Manual, Westinghouse R&D Center, 1310 Beulah Road, Pittsburgh, PA, 15235.
- [1–16] Soloman, H.D., "Low Cycle Fatigue of Surface Mounted Chip Carrier/Printed Wiring Board Joints", AFWAL-TR-89-4004, September 1987.
- [1-17] Conversation with Bruce C. Steffens, Staff Stress Engineer, Martin Marietta Electronic Systems, 1990.
- [1–18] Subramanyam, S. and Rolph, W.D., "Thermal Analysis of Direct Chip Mount Electronic Systems Using ADINA-T," Computers & Structures, Vol. 32, No. 3/4, pp. 853–859, 1989.
- [1-19] Schroen, W.H., Blanton, P.S., and Edwards, D.R., "Finite Element Analysis of Semiconductor Devices," Presented at the 9th Annual IEE/AESS Dayton Chapter Symposium, 30 November 1988.
- [1–20] Lau, J.H. and Harkins, C.G., "Thermal Stress Analysis of SOIC Packages and Interconnections," IEEE Transactions on Components, Hybrids, and Manufacturing Technology, Vol. 11, No. 4, December 1988.
- [1–21] Lau, J.H., Harkins, C.G., Rice, D., Kral, J. and Wells, B., "Experimental and Statistical Analysis of Surface-Mount Technology PLCC Solder-Joint Reliability," IEEE Transactions on Reliability, Vol. 37, No. 5, December 1988.

- [1-22] Steinberg, D.S., "Tools Available for Implementing AVIP," Presented at the 9th Annual IEEE/AESS Dayton Chapter Symposium, 30 November 1988.
- [1-23] Company Literature, Pacific Numerix, 1200 Prospect Street, Suite 300, La Jolla, CA, 92037, (619) 587-0500.
- [1-24] Conversation with Mark Tinges, Pacific Numerix, 1989.
- [1-25] "USAF ATA Initial Avionics Integrity Assessment," McDonnell Aircraft Company/General Dynamics Fort Worth Division, Doc. No. 86PRO579, 18 December 1989.
- [1–26] Kallis, J.M., "Electronics Reliability Fracture Mechanics", Presentation at the 2nd Workshop on the Application of Fracture Mechanics to Microscale Structures of Modern Electronics, El Segundo, CA, May 1990.
- [1–27] Burkhard, A.H., Kallis, J.M., Duncan, L.B., Kanninen, M.F., and Harris, D.O., "Application of Fracture Mechanics to Microscale Phenomena in Electronic Assemblies." Proceedings of the 7th International Conference on Fracture (ICF7), Houston, TX, 20–24 March 1989.
- [1-28] Conversation with Dr. David T. Read, US Department of Commerce, National Institute of Standards and Technology, Materials Reliability Division, Boulder, CO.
- [1-29] Bhungalia, A., and Kurylowich, G., "Correlation/Validation of Finite Element Code Analyses for Vibration Assessment of Avionic Equipment," WRDC-TR-89-3110, December 1989.

# Chapter 2 **ELECTRONIC MATERIAL PROPERTIES**

### 2.0 Introduction

The purpose of this chapter is to identify the physical properties of materials commonly used in the production of electronic hardware. These properties are necessary inputs to finite element analyses used to calculate thermal distributions, relative deformations and environmentally induced stresses and strains. These properties fall into the following two classifications.

- 1) Thermal The primary properties in this classification are thermal conductivity and the coefficient of thermal expansion (CTE). Where appropriate, the temperature at which a material changes state was identified if these temperatures can be expected in the normal operating range of electronics.
- 2) Mechanical This classification encompasses numerous properties including tensile strength, shear strength, modulus, density, Poisson's ratio, stress cycles to failure curves, shear stress cycles to failure curves, strain/effective strain/shear strain cycles to failure curves, stress vs. strain curves, etc.

For the purposes of this Chapter, a failure mechanism is defined as the property by which a material will fail. These mechanisms include ductile fracture, brittle fracture, fatigue and buckling. A failure mode is the identifiable result of the failure mechanism, ie., a cracked solder joint. Failure mechanisms, which can be addressed by finite element methods, appropriate for each material were identified. The failure modes of electronics, based upon the failure mechanisms of the material, were then identified. Based upon the preceding definitions and the scope of this report, failure mechanisms induced by chemical reactions, processing defects and electrical overstress were not identified.

#### 2.1 Failure Mechanisms and Failure Modes

Figure 2-1 is an illustration of typical line replaceable unit (LRU). The failure mechanisms and failure modes have been identified for the printed circuit board (PCB), the housing (or chassis), the component and the component to PCB interface. In addition,

the type of analyses which finite element methods can perform on each part of the LRU has been identified under the heading "Other". Table 2-1 identifies the environments and forces which are responsible for the failure mechanisms. Table 2-2 identifies material characteristics and the type of FEA analyses that should be performed on the material based on their application, characteristics and failure mechanisms.

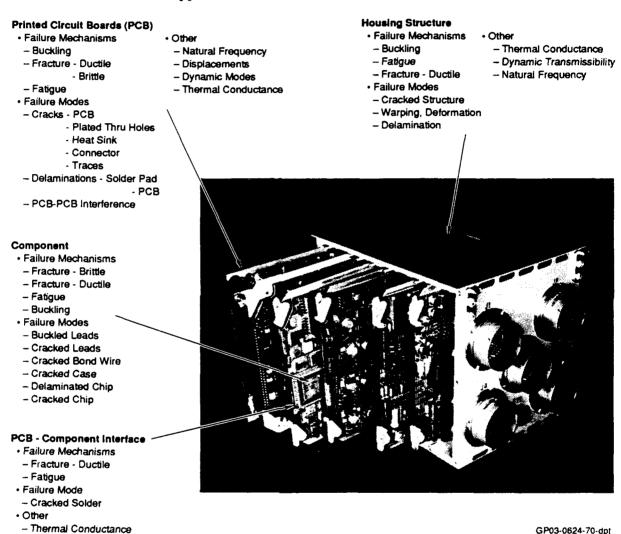


Figure 2-1. "Black Box" Failure Modes & Mechanisms

TABLE 2-1. PREDOMINANT FAILURE MODES

		Force			Failure Mo	echanisms	<del></del>	Envir	onment
Failure Mode	Tension	Shear	Rotational	Buckling	Rupture	Creep	Fatigue	Temp	Vibration
Cracked Solder	х	Х	Х		х	x	X	Х	х
Cracked Lead	х	X	x	x	x		×	х	x
Lifted Pad		X	x		x		[	х	
Cracked Trace	x	X			x			x	
Cracked Via	x				x		×	x	
Cracked Chassis	×	X	x	x	x	x	×	x	×
Cracked Bond Wire	×				x		×		×
Cracked Die Bond	×	x			x		x	х	×
Cracked Die	×				х			x	
Cracked Carrier	×	x	x	x	x			x	×
Cracked Lid Seal		x			x			x	×
Cracked Lead Seal		X		· !	x		×	x	x

GP03-0624-27-D/ks

TABLE 2-2. MATERIAL APPLICATION AND FAILURE MODES

Material	Failure Mechanism	Characteristics	Application	Failure Mode
Metals	Rupture, Fatigue Buckling	Ductile	Housing	Cracks, Warping, Permanent Distortion
			PCB Thermal Plate	Delamination From Dielectrics, Interference With Adjacent PCB, Cracks
			Leads	Cracking, Distortion
			Plated Thru Holes	Cracking
Solder	Rupture, Fatigue	Ductile, Creep	Chip to PCB Interface, Die Attachment	Cracking
Organic Resin	Rupture, Buckling	Brittle	PCB	Delamination From Conductors, Thermal Plane; Distortion; Cracking
Ceramics	Rupture	Very Brittle	Chip Housing, PCB	Cracking
Semiconductor	Rupture	Very Brittle	Integrated Circuits	Cracking

# 2.2 General Material Properties

This section contains the various material properties necessary to perform finite element analyses. Tables 2–3 and 2–4 are a collection of many materials and properties. The data in Table 2–3 was collected from many sources, while Table 2–4 is an excerpt from Reference 2–1. Data in these tables includes both thermal and mechanical properties. Ranges are indicative of the values reported by different sources, a result of the literature search approach to data collection. Table 2–5 is a listing of the CTEs of various materials. Figure 2–2 illustrates CTE information in a manner which allows rapid identification of materials with similar values. Table 2–6 (Ref. 2–2) contains data on the numerous types of laminates and heat sinks used in PCBs. Information includes the glass transition temperature, the CTE in all planes, thermal conductivity, the elastic modulus and the density.

TABLE 2-3. GENERAL MATERIAL PROPERTIES

							m)	
Material	_	Conductivity	TCE	Tensile	Yield	Modulus of	Elongation %	Density lb/in.^3
		ft*deg F	parts per	Strength	Strength	elasticity	in/in	(b) in. 3
	X-Y Axis	Z Axis	million	(KPSI)	(KPSI)	(*10^6)		
Air	0.017							
Acrylic Conformal Coat	0.1		50-90	2.5	2			
Alloy 42	8.8		4-5.3	68	35	21	43	0.291
Aluminum	99-128		10.4-23.8	32	2 <b>8</b>	10	15	0.098
Ве	87		11.5			42		0.067
BeQ (95%)	120		6.4-7.2	13.5	*24.18	39	0.036	0.103
Boron(20%)-Aluminum	100							
Carbon Fiber Epoxy			5- 2					
Ceramic (Al203 96%)	9.6-10.4		5.5-7.5	25-30	28.45	38.5-40	0.063	0.135
Copper	227		17-18	32	4.8-10	17	45-60	0.323
Cu-In-Cu (12.5-75-12.5)	62	8	2.8-3.5	64	38	19	36	0.3
Cu-In-Cu (16-68-16)	81	9						
Cu-In-Cu (20-60-20)	76-95	9	5.0-6.3	56	32	19	36	0.305
Cu-Moly-Cu (13-74-13)	120	92	5-6.5			39		0.357
Ероху	0.13		60	8		0.5		0.066
Epoxy Glass	.172		12.4	40		2.5		.065092
Epoxy Kevlar	0.13		5.7-10			3.5		0.054
Fluorinated Ethylene Propy	0.12		26	2				0.078
Gallium Arsenide	31		5.7		6.1	173		0.192
Germanium	38.5		6.066			18.8		0.199
Glass	5.8		8.6					
Glass Fiber (SiO2)	0.91		.56-5	60		10.5		0.079
Gold	173		14.2	18		10.8	30	0.698
Gold Wire	173		14.2	24	10	10	1-12	0.698
Gold/Silicon	173		9.8	18		10.95	30	0.698
Graphite Epoxy Al	90-100		6.4-10.7					
Graphite(75%)/Cu(25%)	147		5.6			17.5		0.131
Indium	50		32.1	0.38		1.57	22	0.263
Kevlar Fiber			-4-(-2)					
Kovar	14		5.0-5.9	75	50	20	30	0.302
Molybdenum	81		5	95	80	47	10	0.369
Nickel	53		13.3	50	37			0.322
Parylene Conf Coat			35-70	8.2	6			
Polyimide	.006	<b>i</b>	40			0.4		0.063
Polyimide Glass	0.17-0.35	•	11-14.2	50		2.5 - 3.0		.066090
Polyimide Kevlar	.1315	i	3-7	30		3.0-4.0		.052060
Polyimide Quantz	.133		5.0-10					.070061
Polyurethane Conf Coat			100-200					
Polyvinyl Chloride	.071		15-18	4.5				0.057
Quartz Fiber			0.54					
Siticon	72.6	1	2.3-4		5	23.7		0.084
Silver	243	;	19.7	18.13	8	10.3	48	0.379
Solder	25-30	1	21.4-24.6	2.7-7.8	0.34	4.49	37	0.3
Steel (low C)	27	•	10-11			30		0.283
Thermoplastic Resin			25-30					
Tungsten(75%)/Cu(25%)	175	i				38		0.49
•								

<sup>\*</sup> Modulus of Rupture

TABLE 2-4. GENERAL MATERIAL PROPERTIES - 2

	Туре	Material	Temp	k	Cr.	CTE	Ε	G	٧	p	e	Ftu	fsu	Ft ·
C.ass	1 y pe	Hater rat	C	W/in*C	J/16*C	ppm/c	mesi	msi	•	pci	x.	ksi	ksi	ksi
					•	,,				·				
Metal	Pure	Au	25	8.07	58.05	14.20	11.31	3.98	0.42	0.70	30.00	14.94	10.01	nit
Metai	Comp.	4-	23	2د. ،	55.41	14.20	10.50	وبادو	0.42	0.70	οÙ. Θυ	18.00	12.00	r II
Metal	Wire	Au	20	7.62	59.41	14.20	10.00	3.52	0.42	0.70	1-12	24.00	16.08	10.00
Metal	Wire/hard	Au	20	7.62	59.41	14.20	10.80	3.80	0.42	0.70	.5-2.5	62.00	41.54	\$0.00
Metal	Alloy	Au-Si	20	7.62	59.41	9.80	10.95	4.21	0.30	0.70	30.00	18.00	12.06	nil
Metal	Alloy	Au70-Pt30	20	8.07	58.05	14.20	16.51	5.81	0.42	0.72	50.00	92.70	62.11	
Metai	Pure	Ag	50	10.87	106.58	19.00	10.30	3.76	0.37	0.38	48.00	18.13	12.14	8.00
Metal	Comm	Ag	0	106.34	106.12	20.61	10.30	3.75	0.38	0.38	48.00	22.00	14.74	8.00
Metal	Pure	At or At 1199	25	6.27	408.16	23.60	8.99	3.63	0.24	0.10	50.00	50.00	35.00	20.00 4.00
Hetal	Comm	AL 1060	20	5.94	408.16	23.60	10.00	3.76	0.33	0.10	43.00 0.5-5	10.00 34-62	7.00 23-42	27-50
Metal	Alloy	At 1%St or Mg	20 20	5.94 2.49	408.16 104.31	23.60	9.00 7.98	3.76 2.78	0.33	0.10 0.31	50.00	10.30	6.82	27-30
Metal	Pure Elec	Cd Cr	20	1.70	208.53	31.30 6.20	0.04	2.70	0.33	0.26	0.00	12.04	8.06	
Metal Metal	Pure	Cu	20	10.11	175.06	16.50	18.13	6.73	0.34	0.32	60.00	30.30	20.30	4.83
Metal	AS-plated	Cu/CuSO4 bath	20	10.11	175.06	9.50	16.00	5.96	0.34	0.32	15-35	25-35	17-23	25.00
Metal	Plate	Cu/CuSO4 bath	20	10.11	175.06	9.50	10.00	3.72	0.34	0.32	15-35	25-35	17-23	25.00
Metal	AS-plated	Cu/fluroborate	20	10.11	175.06	9.28	12.00	4.47	0.34	0.32	15-32	28-38	19-25	28.00
Metal	Plate	Cu/fluroborate	20	10.11	175.06	9.28	6.00	2.23	0.34	0.32	15-32	28-38	19-25	28.00
Metal	Pure	Pd	20	1.93	111.11	11.76	16.30	6.13	0.33	0.43	30.00	25.00	16.75	5.00
Metal	Pure	in	20	2.20	105.67	32.10	1.57	0.59	0.33	0.26	22.00	0.38	0.25	
Metal	Conen	Ti	20	0.52	237.30	8.82	15.50	6.50	0.19	0.16	24.00	35.00	18.38	25.00
Metal	Alloy	KOVAR	25	0.44	233.50	5.86	20.00	7.59	0.32	0.30	30.00	75.00	50.25	\$0.00
Metal	Comm	Pt	20	1.81	59.86	9.10	24.80	8.92	0.39	0.78	30.00	18.00	12.06	2.00
Metal	Pure	Ní	100	2.11	213.61	13.30	30.02	11.02	0.31	0.32	30.00	45.97	30.80	8.60
Metal	AS-plated	Ni-diff baths	20	2.13-2.78	213.61	13.60	21-31	8-11.8	0.31	0.32	5-35	50-152	33-102	33.00
Metal	Alloy	N170-0r30	20	0.36	208.83	12.20	24.00	9.00	0.33	0.29	30.00	128.00	85.76	
Metal	Alloy	wi50-Fe50	20		218.36	8.46	24.00	9.00	0.33	0.30	0.30	72.00	48.24	
Hetal	Comm	Sn-betta	25	1.54	9.98	23.10	6.40	2.41	0.33	0.26	53.00	1.30	0.87	
Metal	Pure	Mo	20	3.61	125.17	5.22	47.00	17.80	0.32	0.37	10.00	95.00	63.65	80.00
Metal	Pure	Ph	20	0.89	58.50	29.30	2.00	0.69	0.44	0.41	47.00	2.00	1.82	
Metal	Alloy	Sn63-Pb37	20	1.29	165.50	21.40	4.49	1.60	0.40	0.30	37.00	7.80	5.40	0.34
Metal	Alloy	Sn5-Pb93	20	0.89	60.70	28.40	2.68	0.94	0.42	0.39	45.00	4.00	2.10	0.20
Ceramic	96% 99%	A1203 A1203	20	7.87	399.09	7.10	<b>40.00</b>	16.39	0.22	0.14	0.06	25.00	16.76	28.45
Ceramic Ceramic	Sapphire	A1203	20 100	9.84	399.09 341.55	6.50	40.00	16.39	0.22	0.14	0.08	30.00	20.10	28.45
Ceramic	Diamond	C C	20	0.64 50.80	341.33	8.00	50.00	21.50 21.00	0.00	0.14				65.00
Ceramic	Comp	ALN	20	55.12	317.46	0.80 4.10	114.00 40.00	16.00	0.20 0.25	0.12	0.07	28.00	18.76	56.90
Ceramic	Comm	SiC	20	27.56	362.81	3.80	59.00	25.65	0.15	0.12	0.04	26.00	17.42	34.02
Ceramic	Comm	BeO	20	102.36	453.51	7.20	38.00	14.18	0.34	0.10	0.04	13.50	9.05	24.18
Ceramic	KP Grade	BN	20	23.62	294.78	0.00	6.20	2.52	0.23	0.07	0.11	6.50	4.36	7.59
Cermaic	Fused Silica	\$102	20	0.04	357.30	0.56	10.50	4.53	0.16	0.08	••••	0.50	4130	
Ceramic	Corn 7052	Borosilicate	20	0.03	436.43	5.00	8.20	3.36	0.22	0.08	0.12	10.00	6.70	6.00
Ceramic	Corn 9606	Pryoceram	20	0.09	442.33	5.76	17.30	7.09	0.22	0.09	0.08	13.00	8.71	20.00
Ceramic	CERMET	70A1203-30Cr	25			8.65	52.30	33.00	0.21	0.17	0.07	35.00	23.45	55.00
Ceramic	CERMET	77Cr-23A1203	25	1.28	303.40	8.93	37.50	17.00	0.21	0.21	0.06	21.00	40.00	45.00
Ceramic	Forsterite	2MgO-\$102	20	0.03		9.80	21.00	8.54	0.23	0.10				23.00
Semiconductor	Comm	GaAs	20	1.37	10.36	5.70	12.30	4.77	0.29	0.19				6.10
Semiconductor	Comm	Si	20	3.19	341.55	2.33	23.70	9.63	0.23	0.08				5.00
Semiconductor	Corres	Ge	20	1.69	140.48	6.07	18.80	7.34	0.28	0.20				
Polymer	Kapton H	Polyimide film	23	0.00	494.33	20.00	0.43	0.16	0.34	0.05	75.00	25.00		10.00
Polymer	Comm	Polyimide -	23	0.01	494.33	40.00	0.40	0.17	0.33	0.06				
Polymer	Comm	Ероху	23	0.01	800.00	60.00	0.50	0.19	0.35	0.07		8.00	2.00	
Polymer	Cast Rigid	Ероху	23	0.01	854.29	59.40	0.45	0.17	0.35	0.04	4.40	9.50	6.37	
Polymer	Epoxy-conduct	Ablebond 84	23	0.05	333.00	55.00	0.82	0.31	0.33	0.09			1.60	

### Where:

k = thermal conductance

Cp = Specific Heat

CTE = coefficient of thermal expansion

E = modulus of elasticity

G = modulus of rigidity

V = poisson's ratio

P = density

e = elongation

Ftu = tensile ultimate strength

Fsu = shear ultimate strength

Fty = tensile yield strength

TABLE 2-5. CTE FOR ELECTRONIC MATERIALS

Material	CTE	Material	CTE
	ppm/C		ppm/C
411.04 42	5.8	Motybdenum	4.9
Alumina 94%	6.4	Monet	14
Alumina 96%	6.4	Mullite	2.3
Alumina 99,5%	6.4	Nickel	13-15
Aluminum & Alloys	22-28	Nickel Silver	16.2
BeO 99.5%	6.4	Phosphor Bronze	17.8
Beryctium Copper	17.8	Platinum	8.9
Brass (66Cu,34Z.;	20.3	Polycarbonates	50-70
Cadmium	29.8	Polyimides	40-50
Constantan (45Ni, 55Cu)	14.9	Polyurethanes	180-250
Copper & Alloys	16-18	Porcelain on Steel	11.4
Dynamould 103B (epoxy)	22	RTV	800
Dynamould 1048 (epoxy)	25	Sapphire	4.3
Epoxies	60-80	Silicon	2.3
Glass	8.6	Silicon Nitride	2.3
Gold	14.2	Silver	19.7
Gold-Tin Eutectic	16	Steel, Low Carbon	12
Invar	2	Steel, SAE 1045	15
Iron	11.7	Sylgard	300
Kevlar	-2	Tin	23
Kovar	6.2	Titanium	10
Lead	29	Tungsten	4.5
Lead-Tin Eutectic	21	Zinc	39.7
Magnes i um	25.2		

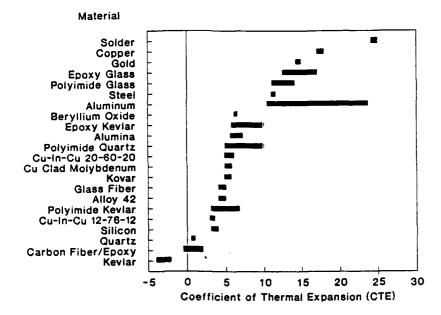


Figure 2-2. CTE for Common Materials

TABLE 2-6. PCB LAMINATE PROPERTIES

Printed Circuit Board Laminates

Material	Glass Transition Tg (C)	CTE x,y	CTE z ppmv°C	Thermal Conductivity (W/m <sup>e</sup> K)	Modulus,Elastic (10E6 psi)	Density (g/cm^3)
E-glass/epoxy	125	12-16	80-90	0.35	2.5	1.8
E-glass/polyimide	200-260	11-14	60	0.35	2.8	1.83
E-glass/PTFE	75	24	261	0.26	0.14	
Kevlar 120W/Quartex	185	3-8	105	0.16	3.2-4.0	1.5
Kevlar 120W/polyimide	180-200	3-8	83	0.12	4	1.44
Kevlar 1201/Quartex	185	0. <i>7</i> 5			6.5	
Kevler 108W/4093 resin	125-135	4-7	50-110		2.3-2.8	
Kevlar 108T/Quartex	185	.75-1.25	66-82		5.5	
Kevlar 2643WW/Quartex	185	5-8	50-110		2.0-2.3	
Quartz/Polyimide	260	6-12	34	0.13	4	1.68
Quartz/Quartex	185		62		2.7	
RO 2800		16-19	24-30	0.44	0.6	
6061 Aluminum		23.6	23.6	190	10	2.71
Copper		17.3	17.3	131	17	8.95
Cu-In-Cu 20-60-20		lateral 6.02	6.02	164	19	8.45
		normal 6.02	6.02	22	19	8.45
Cu-In-Cu 16-68-16		lateral 5.22	5.22	132	19	8.39
		normal 5.22	5.22	19.6	19	8.39
Carith-Cu 12.5-75-12.5		lateral 3.69	3.69	110	19	8.31
		normal 3.69	3.69	17.8	19	8.31
Stee!, low carbon		10	10	27	30	7.84
Atumina 94%		6.4	6.4	21	37	3.6
Cu-Mo-Cu 13-74-13		lateral 6.5	6.5	208	39	9.89
		normal 6.5	6.5	159	30	9.89
8e0 99.5%		6.4	6.4	208	39	2.77
Aluminum, Boron reinforced (20-	50%)	4.5-12.7	4.5-12.7	120-188	12-30	2.0-2.63
Aluminum, graphite reinforced (	40-60%)	32-3.6	32-3.6	310-419		2.41

## 2.3 Solder Properties

This section contains information on solder. Information includes strength properties at various temperatures and cyclic frequencies, cycles to failure based on chip lead count, stress vs. strain curves, cycles to failure based on stress or strain, stress relaxation properties, creep properties and modulus of elasticity variations with temperature and cycle rate.

Table 2-7 (Refs. 2-2,3,4,5) is a summary of solder mechanical and thermal properties. Information includes tensile and shear strength at various temperatures, creep-stresses to obtain a 1000 hour life and thermal conductivity.

TABLE 2-7. SOLDER PROPERTIES

filename	a:CAAR	EM\SOLDER
contains	solder	properties

						Creep :	tress	Thermai
Alloy	Tensile St	rength (PSI)	Shea	r Strengti	n (PSI)	1000 hour	life*	Conductivity
	20 C	100 C	-130 C	25 C	150 C	20 C	100 C	W/m/K
63Sn/37Pb	6120	2700	12700	4130	1165			50.9
60Sn/40Pb	2700	580		4800		4206	653	49.8
50Sn/50Pb	5945		11100	3515	1100			47.8
96.5Sn/3.5Ag	5260		16600	4650	1510			
99\$n/1\$b			15100	2900	1125			
95\$n/5\$b	4410	2900	18150	4625	1880	3046	1305	
10\$n/90\$b	2850	1160	7300	2800	1500			
97.5Pb/2.5Ag			5300	2590	1440			
97.5Pb/1.5Ag/1Sn	4980		5900	3040	1520			
90Pb/51n/5Ag			6220	3470	1755			307

\* Initial creep stress (lb/in2) for life of 1000 hours

Sources:

- Surface Mount Technology; Barbara Roos-Kozel; International Society for Hybrid Microelectronics, 1984.
- Surface Mount Technology; Peter H. Moy; International Society for Hybrid Microelectronics, 1984.
- Soldering in Defense Electronics; K. Nagesh; Bharat Electronics Limited

Figure 2–3 (Ref. 2–6) illustrates cycles to failure data for leadless chip carrier solder joints based upon the number of leads per package. This data was based on a one hour thermal cycle of –55°C to 125°C. Two different substrates were tested. The first PCB was polyimide glass with an aluminum heat sink, resulting in a combined CTE of 15 ppm/C. The second was made of polyimide glass with a CTE of 14 ppm/C. The components had ceramic packages. Figure 2–4 (Ref. 2–7) illustrates a method of predicting cycles to failure based upon the strain factor of the chip–PCB combination. The strain factor considers factors such as CTE, temperature range, chip size and solder height and is represented by the following equation:

$$SF = \frac{L (\alpha_2 - \alpha_1) \Delta T}{2\sqrt{2*h}}$$
 Eq. 1

where:  $\alpha_2 = PCB CTE$ 

 $\alpha_1$  = component CTE

L = component diagonal length

h = solder joint height

 $\Delta T$  = temperature cycle range

□ POLYIMIDE-GLASS BOARD (CTE - 14 PPM/DEG. C)
□ MODULE: P-G WITH AL HEAT SINK (CTE - 15 PPM/DEG. C)

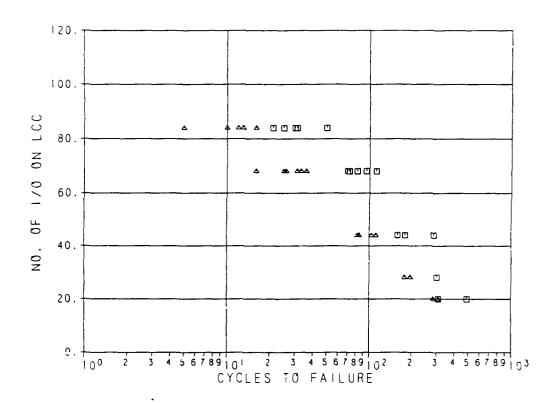


Figure 2-3. Thermal Fatigue Data for LCC Solder Joints by I/O Count

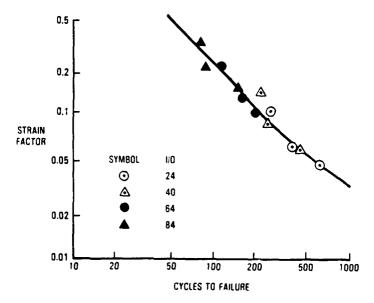


Figure 2-4. Strain Factor vs Cycles to Failure

Figure 2-5 (Ref. 2-8) illustrates the relationship between the principal stress amplitude and the strain amplitude at room temperature. Figure 2-6 (Ref. 2-9) is similar except it plots shear stress as a function of shear strain.

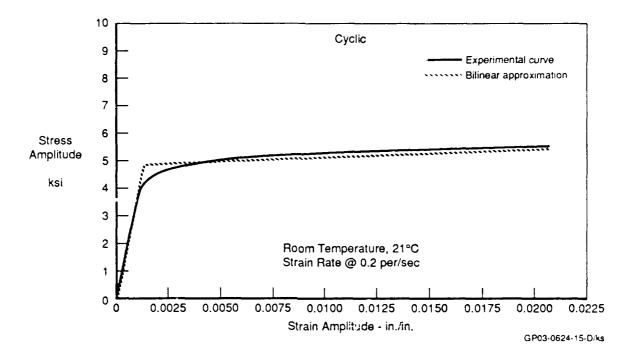


Figure 2-5. Stress vs. Strain for Solder

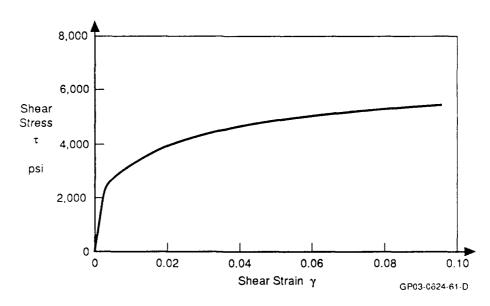


Figure 2-6. Shear Stress-Strain Curve for Solder 63-37

The next group of figures will detail cycles to failure information for solder. Figure 2-7 (Ref. 2-8) plots cycles to failure as a function of principal stress caused by bending for solder which is 50% tin and 50% lead. The figure contains separate slopes for random and constant amplitude stress cycles. Figure 2-8 (Ref. 2-8) is identical to Figure 2-7 except the solder is 63% tin and 37% lead. Figures 2-9 and 2-10 (Ref. 2-8) are identical to Figures 2-7 and 2-8, respectively, except the stress is a fully reversed shear stress instead of a principal stress. Figures 2-11 (Refs. 2-9,10) and 2-12 (Ref. 2-8) also plot cycles to failure as a function of shear stress. Figure 2-12 shows the effect cycle rate and temperature has on the fatigue life of solder. By comparing Figures 2-10, 2-11 and 2-12, variations in recorded material properties becomes obvious, illustrating the importance of carefully choosing data as an input to finite element analyses. The life variations as a function of temperature and stress cycle frequency mandates that the operational environment be correctly quantified. Figure 2-13 (Ref. 2-6) plots cycles to failure as function of shear strain range as opposed to shear stress. This data was collected for polyimide glass PCBs and polyimide glass PCBs with an aluminum heat sink. Figures 2-14 (Refs. 2-9,10) and 2-15 (Ref. 2-7) also plot cycles to failure as a function of shear strain range. Figure 2-15 also plots strain range at various temperatures and cycles rates.

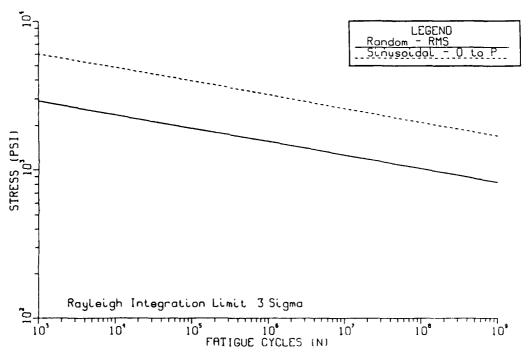


Figure 2-7. S-N Fatigue Curve for Soft Solder (50% Lead - 50% Tin), Reversed Bending

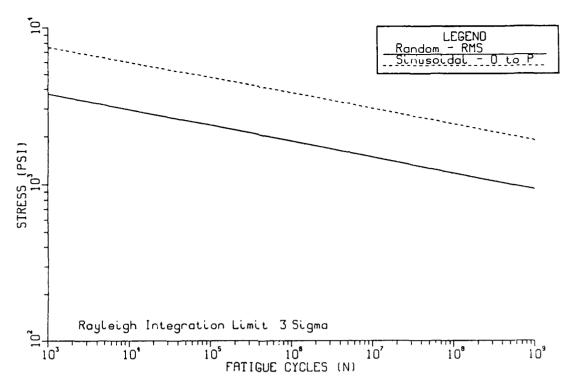


Figure 2-8. S-N Fatigue Cuive for Soft Solder (37% Lead - 63% Tin), Reversed Bending

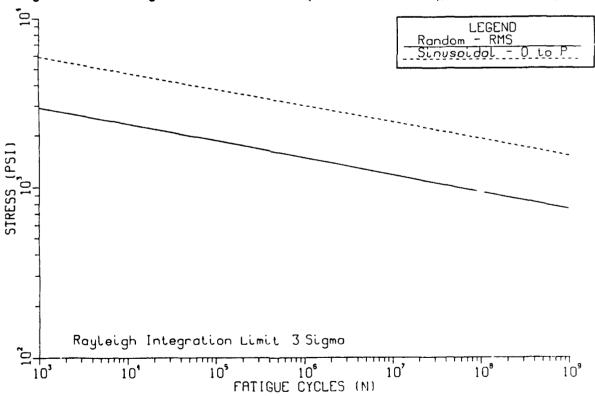


Figure 2-9. S-N Fatigue Curve for Soft Solder (50% Lead - 50% Tin), Reversed Shear

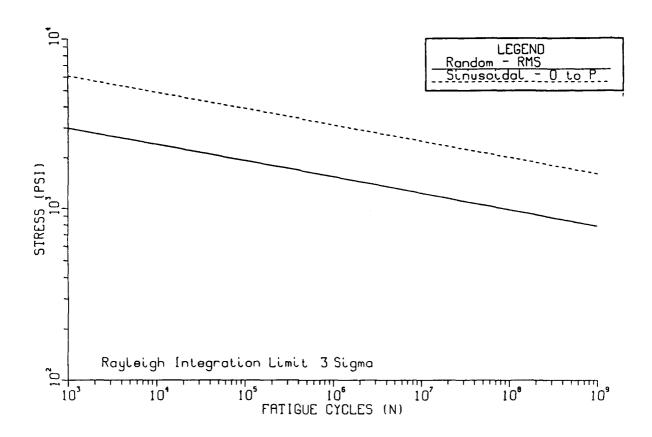


Figure 2-10. S-N Fatigue Curve for Soft Solder (37% Lead - 63% Tin), Reversed Shear

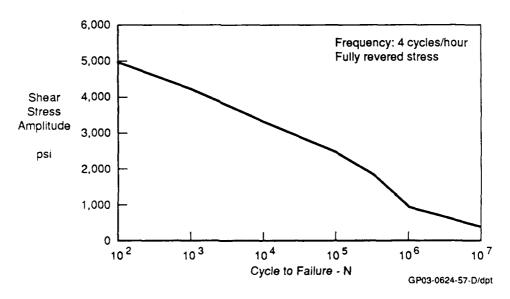


Figure 2-11. S-N Fatigue Curve for 67-37 Solder at Room Temperature

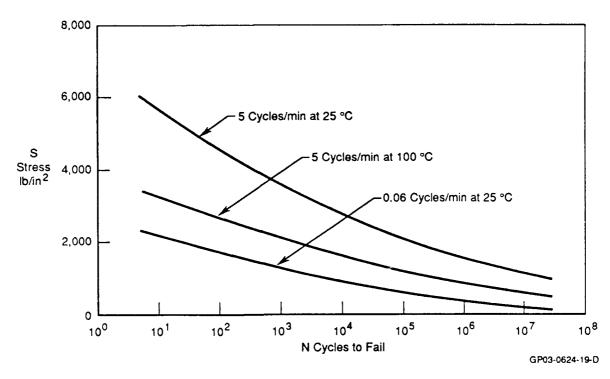


Figure 2-12. Stress vs. Cycles to Failure

(-55 DEG. C - 125 DEG. C; 1 HOUR CYCLE)

POLYIMIDE-GLASS BOARD (CTE - 14 PPM/DEG. C)

MODULE: P-G WITH AL HEAT SINK (CTE - 15 PPM/DEG. C)

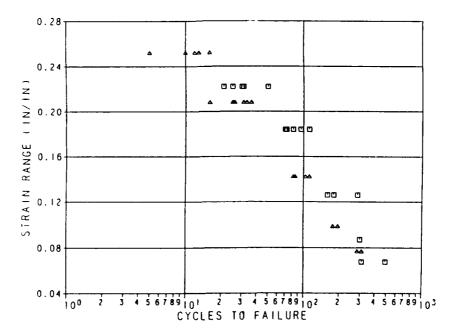


Figure 2-13. Thermal Fatigue Data for LCC Solder Joints

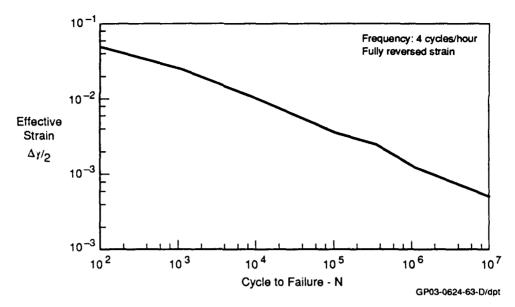


Figure 2-14. Strain-Life Curve for 67-37 Solder at Room Temperature

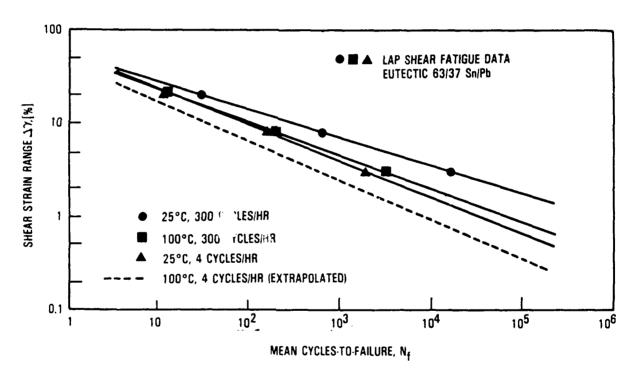


Figure 2-15. Strain Range-Fatigue Life Plots for 63/37 Sn/Pb Solder at Various Conditions

The following set of figures will illustrate a solder phenomenon which raises the level of difficulty in making accurate life predictions – stress relaxation and creep. Stress relaxation occurs when a given strain is imposed on solder. If this strain is maintained, the

stress in the solder will begin to relax or disappear. This continues until the solder is virtually stress free. Creep occurs when a constant stress is applied to solder. The solder will begin to elongate, or stretch, while the stress is maintained. When the stress is relaxed, the elongation does not return to zero. Permanent deformation has occurred. Figure 2–16 (Ref. 2–11) plots remaining stress versus time for 63/37 solder at various temperatures. As shown, the higher the temperature, the quicker the stress relaxes. Figure 2–17 (Ref. 2–10), plots the time to fail for solder subjected to a constant stress. This is plotted for several different temperatures. Figure 2–18 (Ref. 2–10) illustrates the relationship between the speed of the applied stress and the stress to fail. The faster the applied load, the stronger the solder is. Figure 2–19 (Ref. 2–7) illustrates the correlation between the life time of solder and the percentage of creep per cycle.

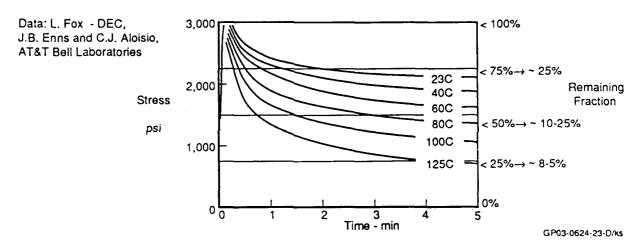


Figure 2-16. Solder Joint Stress Relaxation (63/37 Sn-Pb)

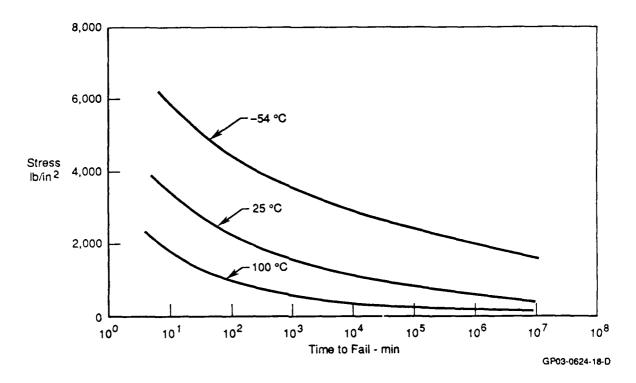


Figure 2-17. Solder Creep Properties

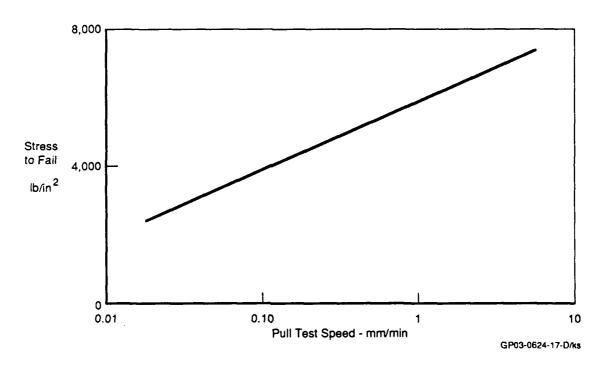


Figure 2-18. Strength vs. Strain Rate

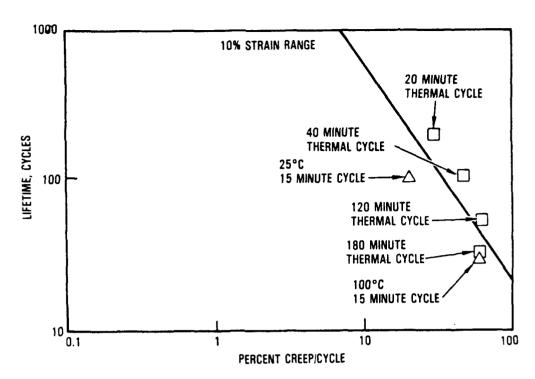


Figure 2-19. Lifetime Data for Eutectic Solder Versus Percent Creep Per Cycle

The last bit of data for solder is shown in Figure 2-20 (Ref. 2-7). It illustrates the relationship between the modulus of elasticity of solder and the temperature and stress cycle frequency. It clearly shows that solder is less elastic at the lower end of the normal thermal range for military hardware. Additionally, it is less elastic at higher stress cycle frequencies.

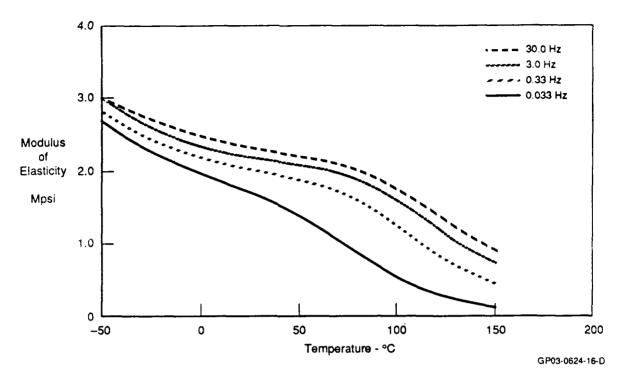


Figure 2-20. Solder Modulus With Temperature

# 2.4 Component Lead S-N Curves

The following group of figures (Figures 2-21,22,23,24) provides stress cycle to failure data for common lead materials. All stresses are principal stresses. This data was collected from Reference 2-8.

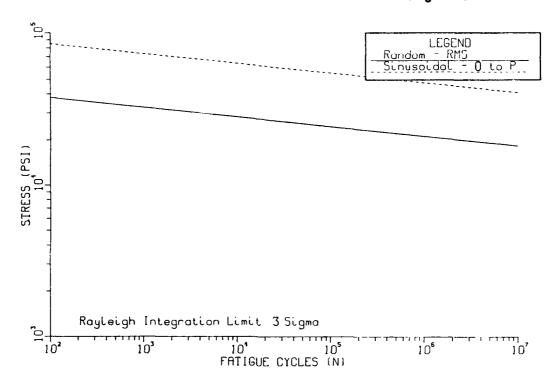


Figure 2-21. Typical Random and Sinusoidal S-N Fatigue Curves for Kovar, Reverse Bending

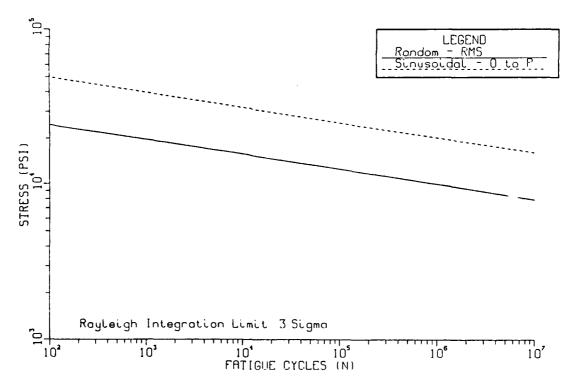


Figure 2-22. S-N Fatigue Curve for Electrical Lead Wire (99.9% Copper Cold Drawn), Reversed Bending

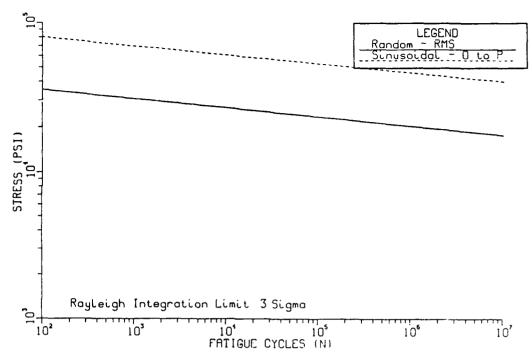


Figure 2-23. S-N Fatigue Curve for Electrical Lead Wire (99.9% Nickel), Reversed Bending

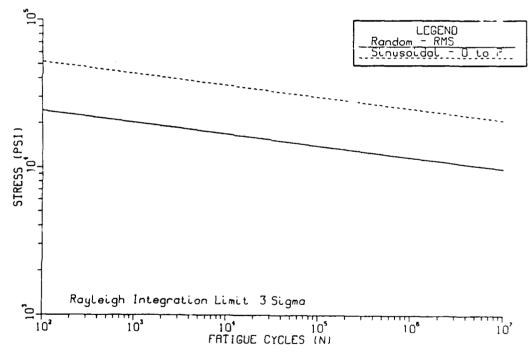


Figure 2-24. S-N Fatigue Curve for Electrical Lead Wire (99.9% Silver Hard Rolled), Reversed Bending

#### References

- [2-1] Kallis, J.M., Duncan, L.B., Van Westerhuyzen, D.H., Sandkulla, D.C., MacFarlane, J.D., Naepflin, H.P., Ingersoll, J.G., Tierney, B.D., McHorney, P.E., Erickson, J.J., and Terrill, K.W., "Reliability Assessment of Wafer Scale Integration Using Finite Element Analysis", Hughes Aircraft Company under RADC contract number F30602-87-C-0118, February 1990.
- [2-2] "Electronic Materials Handbook Volume 1, Packaging"; American Society of Metals International; 1989.
- [2-3] Roos-Kozel, B.; "Solder Pastes"; Surface Mount Technology, The International Society For Hybrid Microelectronics, 1984.
- [2-4] Moy, P.H.; "Solder Application"; Surface Mount Technology, The International Society For Hybrid Microelectronics, 1984.
- [2-5] Nagesh, K.; "Soldering in Defense Electronics"; Bharat Electronics Limited.
- [2-6] Perez, R.; "Avionics Integrity Research, PD 7-712"; McDonnell Aircraft Company, 1990.
- [2–7] Soovere, J., Dandawate, B.V., Garfinkel, G.A., Isikbay, N., Steinberg, D.S.; "Thermal Cycling Reliability Life Model for Avionics"; AFWAL–TR–88–3075, June 1989.
- [2-8] Soovere, J., Dandawate, B.V., Garfinkel, G.A., Isikbay, N., Steinberg, D.S.; "Vibration Reliability Life Model for Avionics"; AFWAL-TR-87-3048, September 1987.
- [2-9] Bae, K., Sprecher, A.F., Conrad, H., Jung, D.Y.; "Fatigue of 63Sn-37Pb Solder Used in Electronic Packaging"; ISTFA, 1988.
- [2-10] Steinberg, D.S.; Technical Report submitted to McDonnell Aircraft Company, 1990.
- [2-11] Engelmaier, W.; "Reliability in Surface Mounted Assemblies: Controlling the Thermal Expansion Mismatch Problem"; Smart IV Conference, 1988.

# Chapter 3 FAILURE MECHANISMS

#### 3.0 Introduction

This chapter describes failure mechanisms caused by mechanical stresses which can be analyzed with finite element stress analysis methods. These stresses are a result of the deformations caused by temperature changes, vibration, shock, and high G aircraft maneuvering loads. These deformations result in material fatigue, creep, fracture, buckling, and eventual component failure. The following paragraphs discuss these failure mechanisms in more detail.

#### 3.1 Deformation

Temperature changes occur during power—on cycles, changes in altitude, coolant temperature fluctuations, and diurnal cycles. Thermal cycles cause materials to expand and contract proportionately to their coefficient of thermal expansion (CTE). Since printed circuit boards and the components mounted on them have different CTEs, they deform by different amounts as the temperature changes (Figure 3–1). This results in stresses in the solder joints and lead wires connecting the components to the boards.

Vibration is caused by ground transportation, engine operation, noise, aerodynamic buffet, or gun fire. Vibration results in out-of-plane deformation of printed circuit poards and high frequency stress cycles in the leads and solder joints of the components. As the board deforms, the leads and solder joints are pulled and compressed as illustrated in Figure 3-1.

Other sources of deformation include shock and high G aircraft maneuvers. Shock is caused by installation of line replaceable units, accidental dropping of equipment, detonations during battle situations, hard landings and collisions. The resulting rapid deformations are similar to those of transient vibration. High G aircraft maneuvers impose steady loads (lasting up to several seconds) on circuit boards during the duration

of the maneuver. The out-of-plane deformations caused by maneuvering loads are similar to the vibration displacements, but at much lower frequencies.

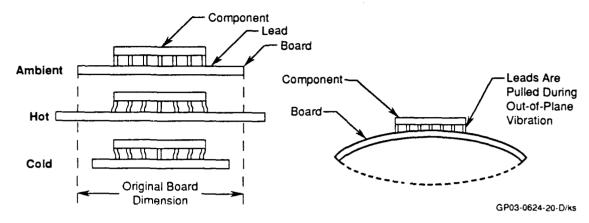


Figure 3-1. Circuit Board Deformation During Temperature Cycles and Vibration

## 3.2 Fatigue

Material fatigue is characterized by the initiation of cracks at areas of high stress following a period of repeated loads. These cracks grow under subsequent load cycles until fracture of the material occurs. The repeated loads are caused by vibration, temperature cycles and the other deformation sources described in Section 3.1. Material fatigue data is typically presented as plots of cyclic stress amplitude versus cycles to failure, commonly referred to as S-N curves (Figure 3-2). As the figure suggests, higher stresses result in shorter fatigue lives. When the stresses exceed the yield strength of the material, failure can occur in relatively few cycles. Fatigue cracks are frequently observed in the solder joints of leadless chip carriers (Figure 3-3) and J-leaded surface mount components (Figure 3-4).

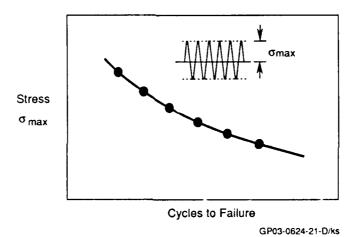


Figure 3-2. Typical Format of Fatigue Data

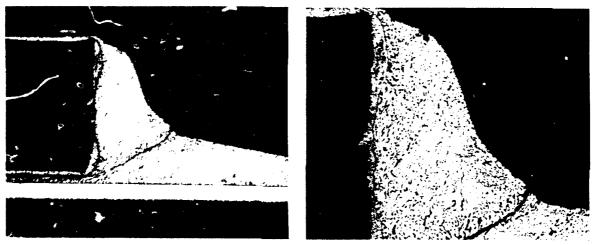


Figure 3-3. Fatigue Crack in a Leadless Solder Joint

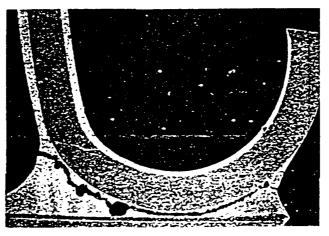


Figure 3-4. Fatigue Crack in a J-Lead Solder Joint

## 3.3 Creep and Stress Relaxation

Under a constant force, materials such as solder will deform with time, or creep. Under a constant displacement, the stress in solder relaxes with time. These conditions are illustrated in Figure 3–5. Models of combined creep and stress relaxation have been developed by Hall (Reference 3–1) and creep data for solder is documented in Reference 3–2.

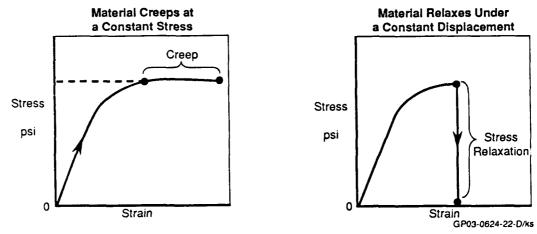


Figure 3-5. Solder Creep and Stress Relaxation Behavior

Stress relazation can occur under the following circumstances. When electrical power is turned on, the components and PCBs heat up and begin to expand. With time, the temperature will reach a maximum. At this point, the stress induced by the CTE mismatch will be a maximum, as will the strain. If power remains on, the strain will remain constant, but the stress will begin to relax. This relaxation can take place quite rapidly (Reference 3-3). Figure 3-6 (Reference 3-4) illustrates stress relaxation versus time for solder at various temperatures. This Figure shows that between 75-95% of stress relaxes within 5 minutes of strain stabilization. This phenomenon will be used to greatly simplify the compilation of load histories (discussed in Chapter 5).

From a finite element modellers point of view, failure is accelerated for the following reasons. As mentioned earlier, when a material which exhibits stress relaxation properties is held at a constant displacement, the stress will dissipate to zero with time. When the displacement returns to the original position, the material will be compressively loaded at a value equal in magnitude to the tensile loading it was under prior to stress

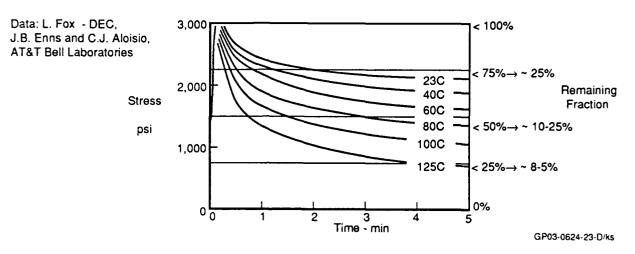


Figure 3-6. Solder Joint Stress Relaxation 63/37 Sn/Pb

relaxation. Therefore, the part has been subjected to a stress amplitude twice as large as a material which does not exhibit stress relaxation (Figure 3-7).

For loading conditions which cause creep to occur, the failure mechanism which can be modelled is the strain amplitude. The strain amplitude, in this case, includes the initial strain (before creep begins) and the additional strain which results from creep. Therefore, the total strain is much greater than for materials which do not creep (Figure 3–8).

Creep can occur when a constant load source is confined by a material such as solder. There are few constant load sources in avionics; however, one situation closely approximates this condition. During manual soldering operations, the leads of gull wing surface mount devices may be held down flush on the pad while the solder is flowing. Once the solder solidifies and the lead is released, a constant force will be exerted on the solder by the lead as it attempts to return to its original position. This could cause the solder to creep.

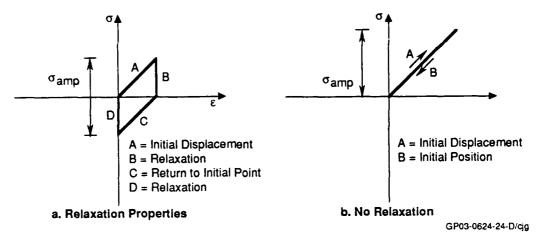


Figure 3-7. Hysteresis Curve for Materials Exhibiting Stress Relaxation

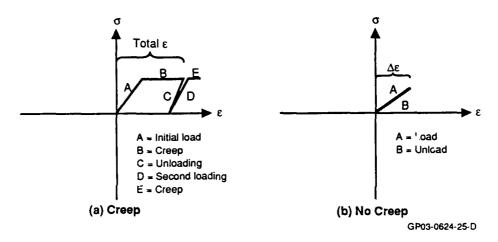


Figure 3-8. Hysteresis Curve for Materials Which Exhibit Creep

#### 3.4 Fracture

#### 3.4.1 Ductile Fracture

Pre-existing flaws and cracks, which initiate under repetitive fatigue cycles, propagate through the material until they reach a critical size. Additional cycles result in fracture. Sustained stresses in solder, for example, can result in creep deformation and eventual rupture. Creep can also act in combination with cyclic fatigue stresses to cause fracture after a given number of stress cycles. A reliability analysis under these conditions requires a fatigue calculation to determine the number of cycles to failure, or a creep analysis to compute the time to failure.

Fracture can also occur immediately if the applied stress exceeds the ultimate strength of the material. If high stresses are limited to a small section of a ductile material such as solder, the material will yield in that region and stresses will be redistributed through the rest of the material (Figure 3-9). As the load is increased, the plastic zone will increase

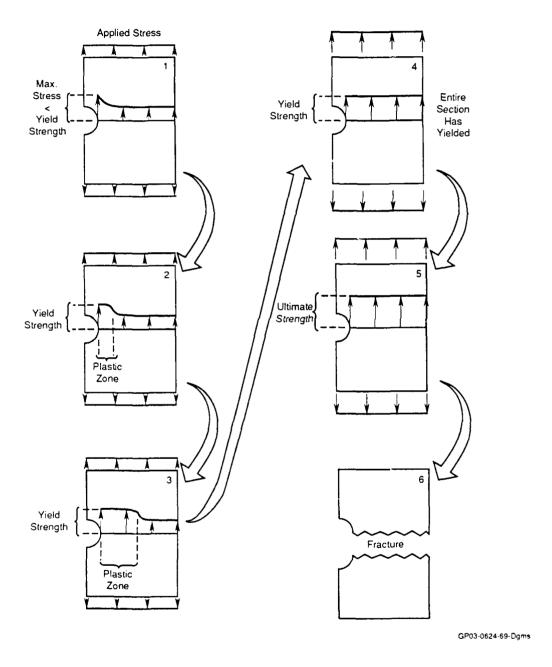


Figure 3-9. Stress Behavior in a Ductile Material as Applied Stress Increases

in size until the entire cross section has reached the yield strength of the ductile metal. If the load continues to increase, and the stress reaches the ultimate strength of the material, rupture occurs.

#### 3.4.2 Brittle Fracture

Brittle materials such as ceramics generally do not yield or undergo plastic deformations. If stresses exceed the ultimate strength of the material in any section of the part, the material will fracture. A reliability analysis must, therefore, include a check of the stress levels in the part to determine if stresses have exceeded the yield strength in ductile materials or the ultimate strength in brittle materials.

### 3.5 Buckling

If a short column is loaded in compression, it will remain straight and the stresses and strains computed in a static finite element analysis are valid. However, a different type of behavior occurs for long, slender columns. When the compressive load reaches a critical level, the slender column will bow out of the plane of its axis, or buckle. The column is unable to carry any further loads because large lateral deflection occurs with little increase in load. Buckling is illustrated in Figure 3–10.



Figure 3-10. Buckling Under a Compressive Load

### 3.6 Failure Modes of Electronics due to Failure Mechanisms

Table 3–1 summarizes the typical failure modes of electronic hardware. Additionally, it correlates the failure mechanisms, types of loading and probable environment with the individual failure modes.

TABLE 3-1. PREDOMINANT FAILURE MODES

	Force			Failure Mechanisms				Environment	
Failure Mode	Tension	Shear	Rotational	Buckling	Rupture	Creep	Fatigue	Temp	Vibration
Cracked Solder	X	Х	х		х	x	x	X	x
Cracked Lead	х	x	x	x	x		×	x	×
Lifted Pad		х	x		x			х	
Cracked Trace	x	x			x			х	
Cracked Via	x				x		×	х	
Cracked Chassis	×	х	x	×	x	×	×	x	×
Cracked Bond Wire	×				x		×		×
Cracked Die Bond	×	х			×		×	х	×
Cracked Die	×				x	ļ		х	
Cracked Carrier	×	х	x	×	x			х	×
Cracked Lid Seal		×			×			х	×
Cracked Lead Seal		x			×	ļ	×	×	×

GP03-0624-27-D/ks

#### References

- [3–1] Hall, P.M., "Creep and Stress Relaxation in Solder Joints in Surface Mounted Chip Carriers," Proc. IEEE 37th Electronic Components Conf., May 1987, pp.579–588.
- [3-2] Becker, G., "Testing and Results Related to the Mechanical Strength of Solder Joints," Presented at the IPC Fall Meeting, San Francisco, CA, September 1979.
- [3-3] Engelmaier, W., "Fatigue Life of Leadless Chip Carrier Solder Joints During Power Cycling," Proc. of the Technical Program of the 2nd Annual International Electronics Packaging Society Conf., San Diego, CA, November 1982.
- [3-4] Engelmaier, W., "Reliability in Surface Mounted Assemblies: Controlling the Thermal Expansion Mismatch Problem," Presented at the SMART IV Conference, Los Angeles, CA, January 1988.

# Chapter 4 FINITE ELEMENT TECHNIQUES

### 4.0 Introduction

Chapter 4 will identify concepts which increase the accuracy of FEAs including techniques addressing mesh generation, model minimization and choice of analyses (linear vs. nonlinear). Example problems will demonstrate FEA accuracy when dealing with very small structures and structures made of materials which have large variations in their elastic modulus. Additionally, example problems will compare FEAs of solder joints (for J-lead and leadless devices) using various FE codes. An example problem will also be used to demonstrate the transfer of PCB deflections into loading on component leads. Before the example problems are discussed, a brief tutorial on finite element analyses will be given. Discussions will cover finite element methods, finite difference methods and hand calculations.

### 4.1 Numerical Methods in Engineering Analysis

Engineers in the electronics industry use a wide variety of modeling techniques to investigate the thermal and structural properties of electronics systems operating in many different environments. Mechanical phenomena typically studied by engineers can be described by the laws of physics in terms of algebraic, differential, or integral equations relating various quantities of interest. While the derivation of the governing equations for most problems is not unduly difficult, their solution by exact methods of analysis is a formidable task. The methods used will often depend upon the complexity of the problem, the time, the manpower, the funds and knowledge of the engineers. The two basic methods of modeling and analysis are generally described as either closed-form or numerical analysis techniques. Closed-form solutions are an easy and efficient form of "hand" calculations. Numerical methods, i.e., finite difference, finite element, boundary element, and statistical energy, enable engineers to analyze structures too complex for closed-form solutions. By far the most common of these numerical techniques is the finite element method (FEM).

#### 4.1.1 Finite Element Methods

In the finite element method, mechanical systems and structures are represented by a discrete grid of node points interconnected by various types of structural elements forming a finite element. The complete solution is obtained by combining the individual elements into an idealized structure for which the conditions of equilibrium and compatibility are satisfied at the nodes of the elements. In the finite element method, the assumed displacement fields within a finite element are assumed, by the use of energy theorems, to derive a stiffness matrix relating the nodal forces to the nodal displacements of the element. If the equilibrium conditions are applied at each node, then a set of simultaneous equations can be assembled and solved for all the displacements in the structure.

As an example, the stiffness matrix for a uniform bar, Figure 4-1, can be derived. Given the governing equation derived from the equilibrium of forces within the bar:

$$\frac{d}{dx}\left(EA\frac{du}{dx}\right) - f(x) = 0$$
 Eq. 1

where f(x) is the internal force per unit length and EA is the elastic rigidity (E is Young's modulus and A is the cross sectional area of the bar). The boundary equations for the problem in Figure 4-1 are:

$$P = EA \frac{du}{dx} \qquad \text{at } x = L$$

$$u = 0 \qquad \qquad \text{at } x = 0$$

$$Eq. 2$$

From the math model in Figure 4-2, the displacement along the length of the bar can be expressed by the unit displacement theorem:

$$u_x = u_1 + (u_2 - u_1) \frac{x}{L}$$
 Eq. 3

The strain in the bar is given by:

$$\epsilon_{\mathbf{x}} = \frac{d\mathbf{u}}{d\mathbf{x}}$$
 Eq. 4

Substituting in the displacement relationship from Eq. 3 yields:

$$\epsilon_{\mathbf{x}} = \frac{1}{L}(\mathbf{u}_2 - \mathbf{u}_1)$$
 Eq. 5

Expressing the strain in vector form:

$$\epsilon_{\mathbf{x}} = \frac{1}{\mathbf{L}} [-1, 1] \begin{bmatrix} \mathbf{u}_1 \\ \mathbf{u}_2 \end{bmatrix}$$
 Eq. 6

Therefore, the strain-displacement relationship is:

$$[b] = \frac{1}{L}[-1,1]$$
 Eq. 7

The stiffness matrix is equivalent to:

$$[K] \simeq \int_{V} [b]^{T} [E] [b] dv \qquad Eq. 8$$

where the [E] matrix is E.

For the problem at hand, the stiffness matrix is:

$$[K] = \int_{0}^{L} \frac{1}{L} \begin{bmatrix} -1\\1 \end{bmatrix} \frac{E}{L} [-1,1] A dx$$
 Eq. 9

After integrating along the length:

$$[K] = \frac{EA}{L} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix}$$
 Eq. 10

For the thermal stiffness, [H]:

$$[H] = \int_{V} [b]^{T} [E_{T}] dv$$
 Eq. 11

Similarly,

$$[H] = -\int_{0}^{L} \frac{1}{L} \begin{bmatrix} -1\\1 \end{bmatrix} EA dx$$
$$= EA \begin{bmatrix} 1\\-1 \end{bmatrix}$$
Eq. 12

The complete force-displacement relationship is:

$$\begin{bmatrix} P_1 \\ P_2 \end{bmatrix} = \frac{EA}{L} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} u_1 \\ u_2 \end{bmatrix} + EA \propto \Delta T \begin{bmatrix} -1 \\ \frac{1}{2} \end{bmatrix}$$
Eq. 13

where a is the coefficient of thermal expansion and  $\Delta T$  is the temperature range.

To complete the problem, discretize the domain (Figure 4-3) and assemble the global stiffness matrix.

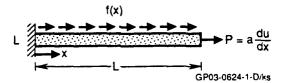


Figure 4-1. Uniform Bar

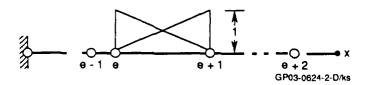


Figure 4-2. Bar Math Model

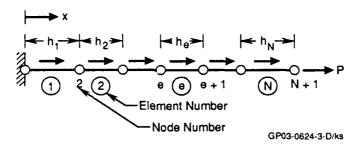


Figure 4-3. Finite Element Idealization

In reality, these structures are continuous systems without grid boundaries. The finite element method is in the form of a mathematical model representing a continuous structure. The analyst must decide upon the model that best represents the structure being examined based upon the type of analysis desired, the time available and the experience of the analyst.

One very important advantage of the finite element method of analysis is that one model can often be used to perform a thermal analysis and a structural analysis. This dual capability makes this technique very powerful since it can dramatically increase the productivity of the design engineer. It is up to the analyst to decide how to properly develop the finite element model to achieve this dual capability. Not all finite element codes are capable of performing both thermal analysis and structural analysis functions. Some of the codes that have dual functions are ANSYS, COSMOS M, STRUDL, NISA, STARDYNE, and NASTRAN. Programs such as STARDYNE and STRUDL only have thermal conduction capability while others also have convection and radiation capability. However, none of the codes have the capability of performing transient thermal analyses where physical properties are mixed. This situation can occur when it is necessary to change radiation and convection relations as a function of altitude and temperature changes, or where there is a change of state from a solid to a liquid that requires using the latent heat of fusion. Problems of this type are easily solved using finite difference methods.

### 4.1.2 Finite Element Computational Process

Most computerized finite element codes break up the computational process into six steps (Reference 4-1). They are:

- 1) Discretization (or representation) of the given domain into a collection of preselected finite elements.
  - a. Construct the finite element mesh of pre-selected elements.
  - b. Number the nodes and elements.
  - c. Generate the geometric properties (e.g., coordinates, cross-sectional areas, etc.) needed for the problem.
- 2) Derivation of element equations for all typical elements in the mesh.
  - a. Construct the variational formulation of the given differential equation over the typical element.
  - b. Assume that a typical dependent variable u, i.e., displacements, is of the form:

$$u = \sum_{i=1}^{n} u_i \ \psi_i$$
 Eq. 14

where  $\psi_i$  are shape functions that satisfy the equilibrium and boundary conditions across the element and substitute it into step 2a to obtain element equations in the form:

$$[K^{(e)}] \{u^{(e)}\} = \{F^{(e)}\}$$
 Eq. 15

- c. Derive or select, if already available in the literature, element interpolation functions  $\psi_i$  and compute the element matrices where:  $K^{(e)}$  is the element stiffness matrix;  $F^{(e)}$  is the force vector; (e) refers to the element.
- 3) Assembly of element equations to obtain the equations of the whole problem.
  - a. Identify the interelement continuity conditions among the primary variables (relationship between the local degrees of freedom and the global degrees of freedom connectivity of elements) by relating element nodes to global nodes.
  - b. Identify the equilibrium conditions among the secondary variables (relationship between the local source of force components and the globally specified source components).
  - c. Assemble element equations using steps 3a and 3b.

- 4) Imposition of the boundary conditions of the problem.
  - a. Identify the specified global primary degrees of freedom.
  - b. Identify the specified global secondary degrees of freedom (if not already done in step 3b).
- 5) Solution of the assembled equations.
- 6) Postprocessing of the results.
  - a. Compute the gradient of the solution or other desired quantities from the primary degrees of freedom computed in step 5.
  - b. Represent the results in tabular and/or graphical form.

#### 4.1.3 General Considerations and Guidelines

A general rule of thumb, as applied to finite element modeling, is that the more elements and node points utilized, the more accurate the model. Many text books show simple problems where improved accuracy is achieved through the use of more node points and some text books show that the stiffness of the model is influenced by the number of nodes and elements, where the fewer the number of nodes, the stiffer the model. In general, there is the desire to use more node points to improve the accuracy. The drawback to using more node points is the rapid increase in the time it takes to solve a large finite element problem. In addition, computer memory requirements also increase rapidly creating problems which cannot be solved on a small machine. A common practice is to use a coarse mesh in areas of the model where accuracy is not important and to use a finer mesh where accuracy is of great importance.

An understanding of the structure to be modeled is critical. It is also necessary to understand how the structure is expected to act when it is exposed to the dynamic environment ic., if bolted covers are used, the structure's stiffness will be altered. Some general considerations in the FEM techniques are outlined below.

- 1) Understand the physical characteristics and properties of the individual building block elements that are available with the particular FEM program being used to develop the model.
- 2) Visualize the geometric shape of the physical system and the general behavior under the action of applied loads and restraints that may distort the geometry.

- 3) Determine the locations of areas that are considered to be critical or areas where information is desired.
- 4) Select the geometry that properly represents the physical structure and its behavior in the environment.
- 5) Select the type of element (solid, shell, beam, plane, etc.) that best represents the characteristics of the structure being analyzed.
- 6) Generate the mesh density that will obtain the desired results in a cost effective manner based upon the capability of the computer being used.
- 7) Apply loading and boundary constraints that are consistent with the geometry and actions of the physical system.
- 8) Utilize previous testing experience or modeling experience to contribute to the understanding of the load path through the structure. Where is the force coming from? Since the force must go to the support or boundary, how does it get there?
- 9) Make use of symmetry to reduce the size of the model.
- 10) Avoid using concentrated loads at a single node point. This can lead to singularities where stress levels are much higher than the true values.
- 11) The shape of the model should approximate the shape of the real structure. If stress levels in a fillet are desired, then a fillet should be included in the model.
- 12) Nodes should be placed at load points and at support poins and anywhere information such as forces, displacements, and stresses are desired.
- 13) A large mesh pattern is desirable in open sections of the model where information is not critical. A gradual change should be made to smaller mesh sizes using a smooth transition.
- 14) Good stress information, in general, requires a finer mesh size than is required for displacement or resonant frequencies.
- 15) Avoid meshing elements with significantly different characteristics, such as solids (which do not bend) with beams or plates that can bend and twist.
- 16) Use curved elements on curved surfaces or use a finer mesh with flat elements at these locations.
- 17) Avoid high aspect ratio (very narrow shell or plate elen ents). Use square shell or plate elements.

18) Gain an understanding of the element behavior and the limitations of the program being used for FEM analysis. This can be done by setting up classic problems where the exact answers exist.

### 4.2 Sources of Errors in a Finite Element Analysis

When a finite element solution converges, it is implied that the exact response of a mechanical idealization has been realized. However, the finite element solution is only an approximation to the exact response and different sources of error affect the finite element solution results. Table 4–1 summarizes the various sources of error (Reference 4–2).

TABLE 4-1. FINITE ELEMENT SOLUTION ERRORS

Error	Error Occurrence In
Singularities	Modeling
Discretization	Use of finite element interpolation
Numerical Integration in Space	Evaluation of finite element matrices using numerical integration
Evaluation of Constitutive Relations	Use of nonlinear material models
Solution of Dynamic Equilibrium Equations	Direct time integration, modal superposition
Solution of Finite Element Equations by Iteration	Gauss-Seidel, Newton-Raphson, quasi-Newton methods, eigensolutions
Round-off	Setting-up equations and their solution

### 4.2.1 Singularities

There is one major source of error that is not well understood by most analysts which can sharply degrade the accuracy of any FEM analysis –singularities. Singularities may produce gross errors in the FEM when stress calculations are requested. Singularities can be found at a point source of heat, a point load, an abrupt change in the boundary, or at a sharp corner in a structure.

Considering a point load, where the theoretical area under the point is zero, the resulting stress level is infinite. The finite elements in the immediate area of the point load

will show artificially high stress levels due to the singularity characteristics. This is not a real condition since all ductile structures will deform slightly until a finite area is formed that will support the load or the structure will fail. However, the computer does not have this information. The first two highest stress levels are often discarded, and the third highest stresses calculated are used to determine the pass and fail criteria for the structure. This is quite arbitrary and not an acceptable practice for evaluating design margins. The accuracy of this type of analysis can be improved by using a nonlinear model where the plastic properties of the material are included in the computer model. The big drawback to nonlinear models is the great amount of computer time that is required to obtain solutions. The analyst must decide if the accuracy improvement is worth the extra computer time required to obtain a solution. Another way to improve the accuracy of the stresses obtained from the application of a concentrated load is to alter the load so it is not applied to a single node point. Spreading the load over a closely clustered group of node points will reduce the singularity effects and reduce the peak stress levels.

Geometric shapes can also result in singularities, especially at holes, notches, angles, and where there are rapid changes in the cross section of a structure. Consider an "L" shaped bracket loaded as a cantilevered beam. When a coarse mesh is used in the finite element model, the inside corner of the "L" will be sharp with zero radius. The stress levels calculated by the computer at this inside corner will be much higher than the true value for the same reasons outlined above. Normal ductile materials will simply plastically deform and relieve the strain so the part will not fail. However, the computer does not have this information unless a nonlinear analysis is performed. One way around this problem is to add a small radius at the sharp inside corner, which will reduce the magnitude of the maximum stresses to a more realistic value.

Singularities will also occur at the boundaries of structural members. When the boundaries are point supports or clamped edges, the conditions can be treated as described above in the section on concentrated loads to avoid singularities.

### 4.2.2 Round-off Errors

Errors critical to the accurate prediction of stress in any general engineering structure such as finite element discretization, have been discussed. Errors critical to the finite element analysis of microelectronic structures, are round-off errors. Round-off errors are a result of the finite arithmetic precision of the computer used. Matrix operations are typically the culprit in introducing solution errors due to round-off, specifically Guass elimination (Reference 4-2). Large solution errors of this type are introduced when the diagonal elements in the stiffness matrix vary by a large amount, or when very smail diagonal elements are used, creating a large multiplier. The reason for the large solution error is the basic mathematical operation in Gauss elimination – factorization. Factorization is a subtraction of a multiple of the pivot row from the rows below it. If numbers of widely different magnitudes represented to a fixed number of digits are subtracted, then the errors in this operation can be relatively large. In other words, if a structure is composed of many different materials, such as a component lead/solder connection, then the soft stiffness of the solder and larger stiffness of the copper lead are represented next to each other in the stiffness matrix. Hence, large and small stiffness values are present on the main diagonal. Another difficulty is analyzing structures where very small dimensions are being modeled. Since refined models are needed to ensure compatibility and completeness of the solution, truncation errors due to numerical precision is very critical. Therefore, using a refined mesh can cause considerable numerical errors if proper precautions are not taken during mesh generation.

### 4.3 Finite Element Accuracy in Stress Analyses

It has been argued that small feature size of electronic devices makes finite element analyses (FEA) inappropriate because of numerical errors. However, these errors can be minimized by following some general guidelines for building the finite element model. The following examples verify numerical errors do not occur when small dimensions are used. Additionally, the ability of FEA to simulate predicted stress concentration factors caused by geometric changes is demonstrated. Finally, a comparison of linear and nonlinear

analyses demonstrates the variation in calculated stresses and strains. The FEA general purpose code ABAQUS was used for these tests.

When utilizing finite element analysis techniques for small scale structures, the following guidelines must be adhered to in order to achieve realistic results:

1) Quadrilaterial elements should be kept as square as possible. The aspect ratios should be maintained as depicted in Figure 4-4. In cases of uniaxial stress fields, larger aspect ratios are acceptable.

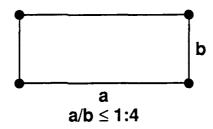
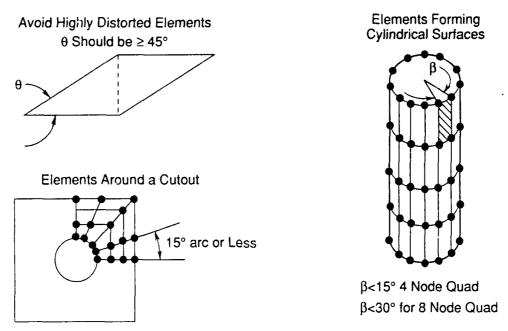


Figure 4-4. Aspect Ratio for Quadrilateral Elements

- 2) When analyzing plates and shells, be sure to provide a sufficient number of elements across the span to follow the deflection surface and the changes in shear. Remember that the analysis replaces the uniform pressure over the element area by a set of equivalent point loads applied at the grids.
- 3) Finite element modeling of small scale structures such as those shown in Figure 4-5, requires finite elements that have been formulated to be less sensitive to curvature or skewed geometries. The accuracy of typical finite elements based on simple linear shape function approximations (typical four node, 20 degree-of-freedom, quadrilateral elements) is very sensitive to modeling geometries; for instance:
  - a. It is essential to keep the relative size of elements in areas of critical stresses the same.
  - b. Elements must also be relatively square in shape (aspect ratio equal to one) in areas of critical stress prediction.



GP03-0183-70-D

Figure 4-5. General Guidelines for Finite Element Modeling

### 4.3.1 Compatibility and Completeness of the Finite Element Mesh

As a general rule of thumb, the more elements or degrees of freedom (DOF), the more accurate the solution. However, when trying to decrease model size but still retain accuracy, a coarse mesh can be used in areas of a structure where stress prediction is less critical. For the finite element solution to converge thru mesh refinement (h-version FEA), it is necessary that the elements that make up the assemblage be complete and compatible. The requirement for completeness of an element means that the displacement functions of the element must be able to represent the rigid body displacements and constant strain states. The refinement of a finite element mesh is required to obtain a constant strain state within an element. If more and more elements are used in the assemblage to represent a structure, each element approaches a very small size and the strain in each element approaches a constant value. The complex variation of strain within the structure can then be approximated. The requirement of compatibility means that the displacements within the elements and across the element boundaries must be continuous since the stresses in an element are calculated using derivatives of the displacement.

When calculated in adjacent elements, the stress may vary substantially if a coarse mesh is used or if adjacent elements are not the same size (as when transitioning from a coarse mesh to a refined mesh) because force equilibrium has not been satisfied. The stress difference at the element boundaries decreases as the finite element idealization is refined, and in practice, acceptable results are usually obtained if element boundary stresses are averaged.

#### 4.3.2 Small Element Size Effects

The effect of micro-dimensioned finite element models on stress calculation accuracy was examined for a plate with a hole in tension. The model in Figure 4-6 shows the

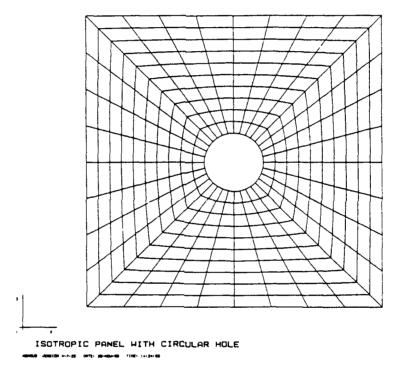


Figure 4-6. Isotropic Panel With Circular Hole

mesh of a square plate with a distributed load along the top and bottom. The overall plate size was varied from 10 inches to 0.0001 inches in length. The predicted stresses were equal for all plate dimensions considered with a gross section stress concentration  $K_t$ , of 3.370. The ratio of the hole diameter (a) to the plate length ( $\ell$ ) was held constant at 0.2 as was the ratio of the plate length ( $\ell$ ) to plate thickness (t), at 100. The loading was proportionally reduced to yield the same nominal stress,  $\sigma_{nom}$ , which is defined as:

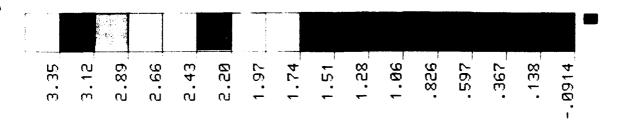
$$\sigma_{\text{nom}} = \frac{P}{\ell t} = 1.0$$
 Eq. 16

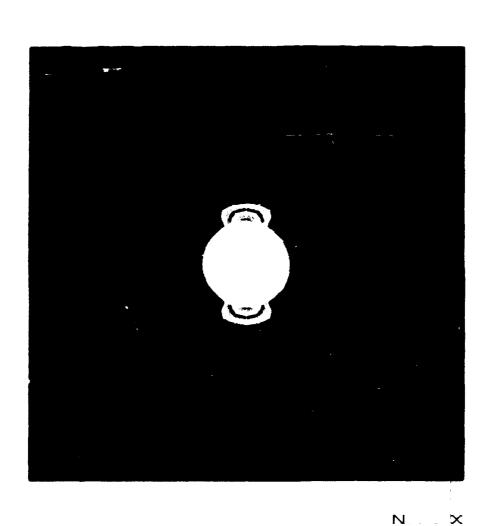
where: l = length

t = thickness

p = load

Therefore, each finite element model was expected to predict the same maximum stress at the hole. Figure 4–7 shows the typical stress distribution around the hole. The finite element results are shown to be within 7% of the 3–D elasticity solution,  $K_t = 3.14$  (Ref. 4–3).





ISOTROPIC PANEL WITH CIRCULAR HOLE
ABAQUS U4-7-25 20-NOU-90 14:48:32
PROCEDURE 2 TIME STEP 1 INCREMENT

Figure 4-7. Isotropic Panel With Circular Hole - FEA Strusses

#### 4.3.3 Beams of Two Materials

The second analysis was a small beam made of two different materials. The beam is illustrated in Figure 4–8. The concern was to accurately predict the stress at the interface between the soft and stiff materials. A stress jump (or discontinuity) will always exist between two adjoining elements. However, as the mesh is refined, the stress jump will diminish (or converge) as long as the original mesh is contained within the new mesh. Following the guidelines mentioned in the previous section, several consecutive refinements in the mesh are made to determine the rate of convergence. The meshes used in this study are depicted in Figure 4–9. Each mesh is a double refinement of the previous mesh. In each successive mesh refinement, the stress jump at the material interface was calculated. Table 4–2 lists the stress jumps for each mesh. As a rule of thumb, a stress jump of 5 percent across the element boundary is considered sufficient refinement.

The mesh used did not have any abrupt element size changes and it did not have any high aspect ratio elements in the area of high predicted stresses. This analysis shows FEA is reliable for stress prediction of objects with varying elastic modulus.

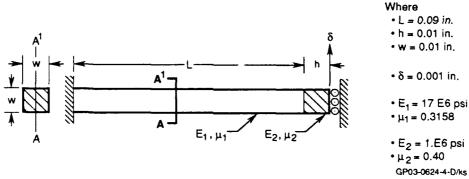


Figure 4-8. Slender Beam With Two Materials and Square Cross-Section

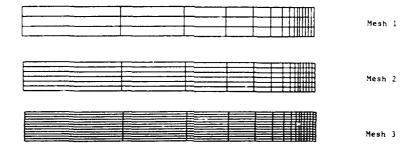


Figure 4-9. Tip Loaded Cantilever Beam With Two Materials - Mesh

TABLE 4-2. INTERFACE STRESS DISCONTINUITIES

Mesh Number	Stress Jump (psi)	Precent Difference
1	1499	10.8%
2	1313	10.1%
3	722	5.6%

### 4.3.4 Comparison of Linear and Nonlinear FEAs

This section discusses a technique which will allow the use of linear FEAs to model situations where plastic deformations occur in the structure. Considerable time savings can be realized with this technique when compared to using nonlinear (or elastic-plastic) FEAs.

If stresses are greater than the yield strength  $(\sigma_{ys})$  of the material, the high stress section of the component is in a plastic state. This condition is characterized by nonlinear stress  $(\sigma)$  versus strain  $(\epsilon)$  behavior is illustrated in Figure 4–10a. The stresses computed by a linear FEA analysis are not valid since a linear relation between stress and strain has been assumed. To compute the actual stress and strain, a nonlinear elastic-plastic FEA analysis can be done, but this is usually complex and time consuming. The actual stress and strain can be estimated very rapidly by using the stress and strain computed by the linear FEA as illustrated in Figure 4–10b. This will give a lower (less conservative) estimate of the actual conditions. Another more conservative estimate can be obtained by using Neuber's rule for notch analysis with a stress concentration of 1.0. This results in:

$$(\sigma \epsilon)_{\text{actual}} = (\sigma \epsilon)_{\text{FEA}}$$
 Eq. 17

The actual stress and strain combination must fall on the curve of  $\sigma$  vs.  $\epsilon$  as illustrated in Figure 4–10c.

A simple test case has been analyzed for the purpose to verify nonlinear methods for stress prediction in microelectronic structures. A two dimensional ABAQUS model has been developed for elastic-plastic analysis and was compared to a linear ABAQUS model for stress prediction. The linear J-lead analysis in Figure 4-11 demonstrates how high

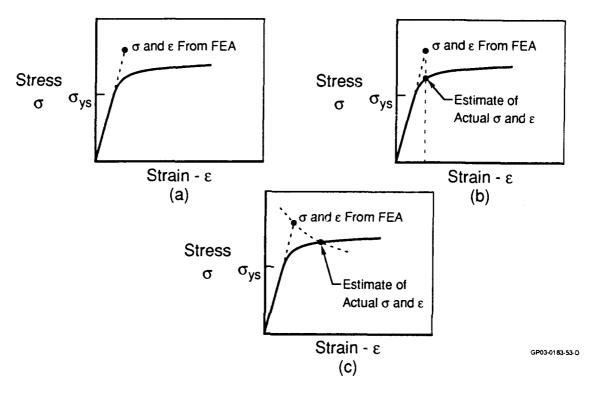


Figure 4-10. Stress and Strain Approximations

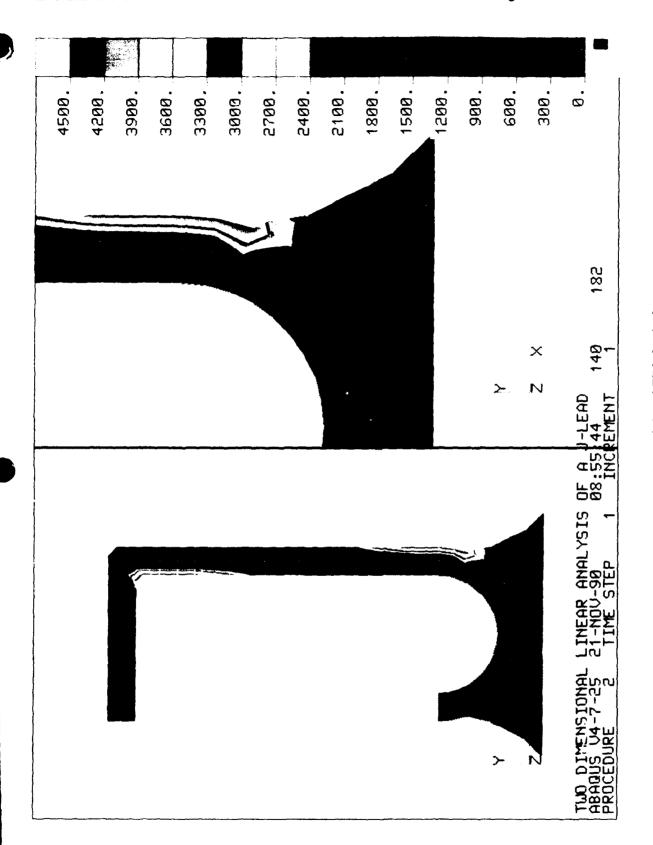


Figure 4-11. Linear J-Lead FEA Analysis

thermal loads can cause yielding in the solder connection for the lead. Stresses in the solder are greater than the yield strength ( $\sigma_{ys}$ ) of the material, as shown in Figure 4–12. The stresses computed by the linear FEA analysis are inaccurate, since, they assume a linear relationship between stress and strain. However, the actual stress can be approximated by dropping vertically down to the material stress ( $\sigma$ ) vs. strain ( $\varepsilon$ ) curve (Figure 4–12a). This linear correction gives a lower estimate of the actual condition. A more conservative estimate was obtained using Neuber's rule for notch analysis with a stress concentration of one. The actual stress and strain predicted by the ABAQUS elastic–plastic analysis falls on the  $\sigma$  vs.  $\varepsilon$  curve between the linear correction and Neuber's rule. For this case the difference in the linear approximation and the nonlinear analysis was minimal. In general, an elastic–plastic analysis can be avoided by checking the difference in strain prediction between the linear correction and the Neuber approximation. For this case, the difference in strain was small ( $\approx$  10%) and would not have made a big difference in the fatigue life.

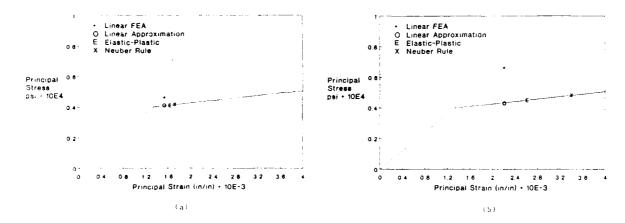


Figure 4-12. Stress - Strain Nonlinearity

For the case when the degree of nonlinearity is great (Figure 4–12b), then an elastic-plastic analysis is critical for accurate fatigue life predictions. The nonlinear analysis is necessary in this case due to the large horizontal error in the strain prediction. In this case, the strains predicted by the linear approximations disagree by more than 50%. This difference can relate to a factor of 5 to 10 difference in the fatigue life.

For both test cases, the vertical error in stress prediction is negligible between the linear approximations and the nonlinear calculation. This shows the importance of using strain versus life data for low cycle fatigue ( $< 10^4$  cycles) as opposed to stress versus life data which is more applicable for high cycle fatigue calculations.

### 4.4 Dynamic Modeling/Analysis Technique for Electronic Equipment

Failures that occur in electronic systems during exposure to vibration environments will usually be associated with PCBs since they support the most sensitive elements of the assemblies. These sensitive elements include the electronic components, their electrical leads, solder joints, plated through-holes, and interface electrical connectors. When the resonant frequencies of the PCB are excited during vibration, the PCB will bend back and forth as shown in Figure 4–13. This flexing action will produce relative motion between the PCB and the electronic component body. When the component has leads for electrical interconnections, the load path will pass through the lead and into the solder joints, the plated through-holes, and into the plastic (usually epoxy fiberglass or polyimide glass) PCB. High acceleration vibration levels and lightly damped PCBs can

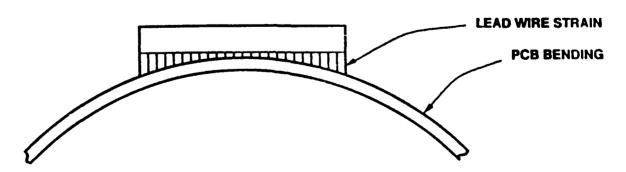


Figure 4-13. Printed Circuit Board Out-of-Plane Displacement

produce large dynamic displacements which will cause rapid fatigue failures in the leads and solder joints. A closer examination of the lead bending displacements in Figure 4–14 shows that the end leads have the greatest movement and the middle leads have the least.

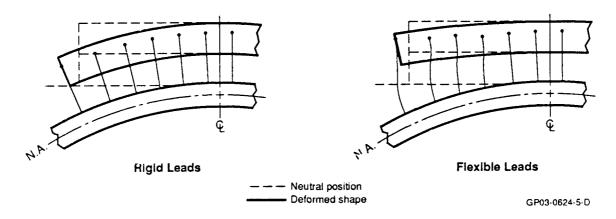


Figure 4-14. Lead Displacement

There are four main components of the electronic assembly which must be modelled: the chassis (or line replaceable unit, LRU); the PCB; the component and leads; and the solder joint connection. The chassis assembly is modeled to establish the magnitude of the dynamic coupling response between the PCB and LRU. The PCB finite element model is used to transfer dynamic displacements and strains onto refined finite element models of the component, lead and solder joint. Use of the these refined models is restricted to determining the stress/strain levels in the leads and solder joints for fatigue life predictions.

### 4.4.1 Determining the Chassis to PCB Dynamic Coupling

Electronic assemblies typically use an outer housing chassis to enclose, support, and protect the PCBs (Figure 4–15). These enclosures will also be excited during the vibration exposure. If care is not exercised during the design phase of the project and the resonant frequency of the outer chassis housing is close to the resonant frequency of one or more PCBs supported within the chassis, dynamic coupling will occur. Under these conditions, the response accelerations and displacements of the PCBs can be further amplified by the resonant conditions of the outer chassis. This coupling between the chassis and the PCB can sharply reduce the fatigue life of the PCB.

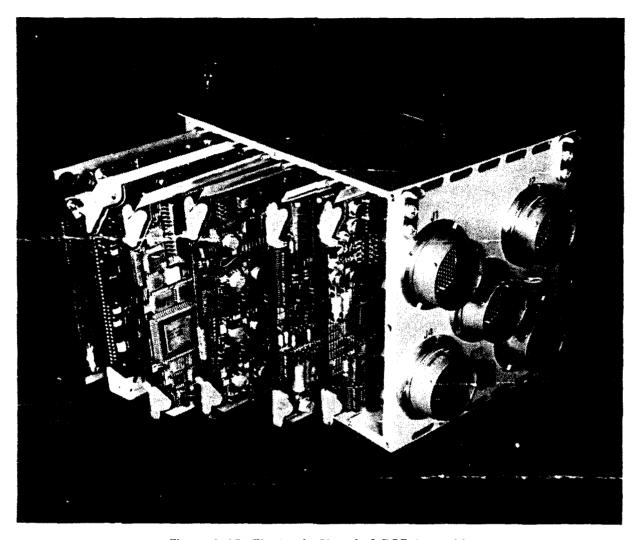
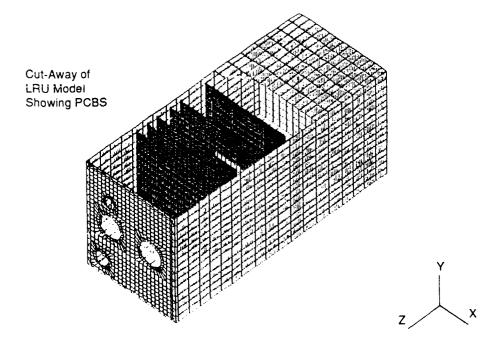


Figure 4-15. Electronic Chassis & PCB Assembly

Therefore, it is essential to establish the magnitude of the dynamic coupling between the LRU and PCB. Hence, the finite element model of the LRU/PCB assembly must consist of an accurate representation of the LRU. In this respect, the finite element model should accommodate cutouts, concentrated masses (power packs), and the compliance between the PCB and the side wall (edge guides and/or wedge clamps). The PCB finite element models included in the LRU model can be simplified to reflect no mass and stiffness effects due to the components. The modes of interest in determining the dynamic coupling are the local panel modes of the LRU side walls and the primary

resonant modes (support modes, and chassis torsion and bending modes). If the LRU chassis is too stiff (which could be the situation when not all mass is represented or when the support mounts on the chassis are not accurately represented), lower than expected PCB vibration levels will result by missing the coupling effect in the analysis. Once the FEM model is complete (Figure 4–16), the computer can be used to determine the frequency response of the assembly. This will show the magnitude of the acceleration levels at every node point in the model across a broad frequency band, typically from 10 Hz to 2000 Hz. The computer can show direct axis response, where a 1.0 G dynamic stimulus is input along the X axis and the response is measured along the X-axis. The computer can also show cross axis response, where a 1.0 G dynamic stimulus is input along the X axis and the response is measured along the Y or Z axis.



GP03-0624-6/gms

Figure 4-16. Chassis Assembly FEM

Steinberg (Ref 4-4) has developed a simple method to approximate the transmissibility factors applicable to the dynamic response of PCBs. If the chassis (LRU) frequency (f<sub>c</sub>) and the PCB frequency (f<sub>p</sub>) are known, the uncoupled PCB transmissibility is given by equation:

$$Q = 1/(1 - R^2)$$
 Eq. 18

where:

$$R = f_f/f_c$$

 $f_f$  = forcing frequency

When the forcing frequency is equal to the natural frequency of the  $PCB(f_p = f_f)$ , the coupled transmissibility is:

$$Q_{p} = Q*SQRT(f_{p})$$
 Eq. 19

Knowing the damping of the PCB and the acceleration levels of the chassis, the coupled transmissibility can be determined.  $Q_p$  accounts for the additional energy from the chassis due to the coupling with the chassis at the  $f_f$  and is the amplification factor applied to the dynamic loads that excite the PCB at the frequency  $f_p$ .

### 4.5 Techniques for Modeling the PCB

Once the LRU to PCB dynamic load transfer is established, the PCB finite element model can be analyzed in more detail by itself. The individual PCB finite element model is used to establish the mode shapes and to determine which components are critical in terms of relative displacement to the PCB. Determining which components are most critical is not a straight forward task. Experience and empirical techniques will minimize the critical components which need to be analyzed in further detail. The PCB is not a critical component by itself since very few failures will occur in the board before the components on the board fail (Ref 4–5.).

The PCB should be analyzed in detail for possible failure of the etched copper traces and for failures of plated through holes (PTH). It is also necessary to predict the individual layer stress distributions. This requires that each layer be modeled with solid finite elements or composite plate-type elements where a composite laminate failure theory can be applied. More commonly, PCBs are modeled with plate-type elements (Figure 4-17) to determine dynamic displacements. Boundary conditions of the PCB can generally be as smed to be simply supported at the mother board connection, unsupported at the top, simply supported on the sides when edge guides (Pircher) are used, or simply supported.

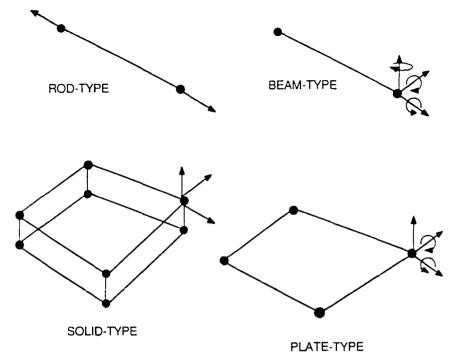


Figure 4-17. Finite Elements for Structural Analysis

with rotation flexibility when wedge guides are used. Steinberg (Reference 4–4) discusses the rotational flexibility of wedge clamp devices. He states that wedge clamps act more like a fixed boundary condition when a PCB's fundamental natural frequency is less than 100 Hz and more like a simply–supported edge when fundamental natural frequency is above 600 Hz. Therefore, if the fundamental frequency is between 100 and 600 Hz, the rotational flexibility or spring stiffness of the wedge guide can be determined by using the relationship:

$$f_n = \frac{f_s + 1.10 (f_t - F_s)}{1 + 0.001 (F_t - f_s)}$$
 Eq. 20

where  $f_n$  = expected natural frequency of PCB

f<sub>f</sub> = natural frequency of PCB with fixed (clamped) sides

 $f_s$  = natural frequency of PCB with simply-supported sides

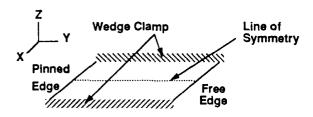
The frequencies  $f_f$  and  $f_s$  are determined from the F.E.A. for a PCB with both fixed sides and simply-supported sides. Then, the expected natural frequency,  $f_n$ , is calculated using the above equation. Using the finite element model, rotational springs are used to

model the wedge guides rotational ilexibility. Therefore, several F.E.A.s are performed at different spring constants until the F.E.A. natural frequency matches the expected natural frequency calculated using the above equation. In other words, the finite element model must be "tweaked" to more closely match a real structure's response.

Component modeling is usually restricted to concentrated mass representation in PCB finite element models. Bivens (Ref 4-6.) showed that the lead design had a negligible effect on the expansion of the component package and the PCB as a result of thermal deflections. A similar behavior can be assumed for dynamic deflections.

When performing a dynamic response analysis of the individual PCB, the symmetry of the structure can be used to reduce analysis cost and effort. For plate type structures, analyzing a quarter symmetry model is limited to a plate with similar boundary conditions on all four sides. Typically, PCBs exhibit only half symmetry (symmetric in only one direction). For a one half symmetry model, it is necessary to perform the eigenvalue extraction two times in order to extract both the symmetric and anti-symmetric modes.

Symmetric boundary conditions about the X plane are specified with  $u_x = \theta_y = \theta_z = 0$ . Anti-symmetric boundary conditions can be specified with  $u_y = \theta_z = \theta_x = 0$  (Figure 4-18). As is typical with PCB structures, the fundamental resonance contributes



PCB is symmetric about the y-z plane.

Boundary conditions along line of symmetry: SYMMETRIC-

 $\begin{array}{ll} U_X\approx \ \theta_Y=\theta_Z=0 & \text{where:} \\ \text{ANTI-SYMMETRIC-} & U - \ \text{displacement degree of freedom} \\ U_Y= \ \theta_X=\theta_Z=0 & \theta \end{array}$ 

Figure 4-18. Printed Circuit Board Boundary Conditions

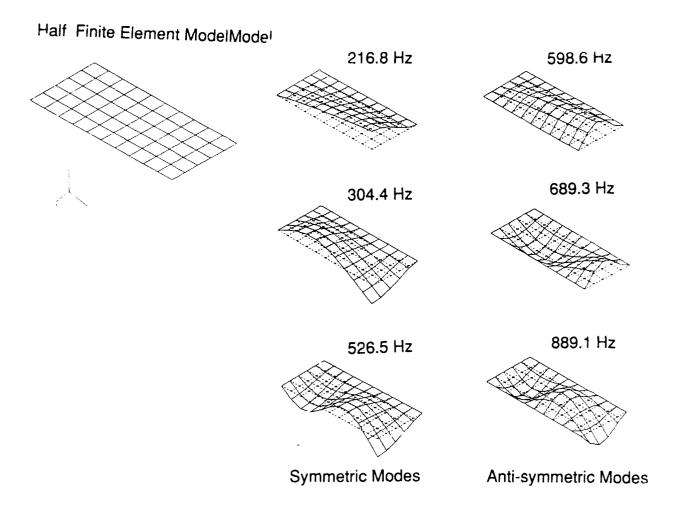
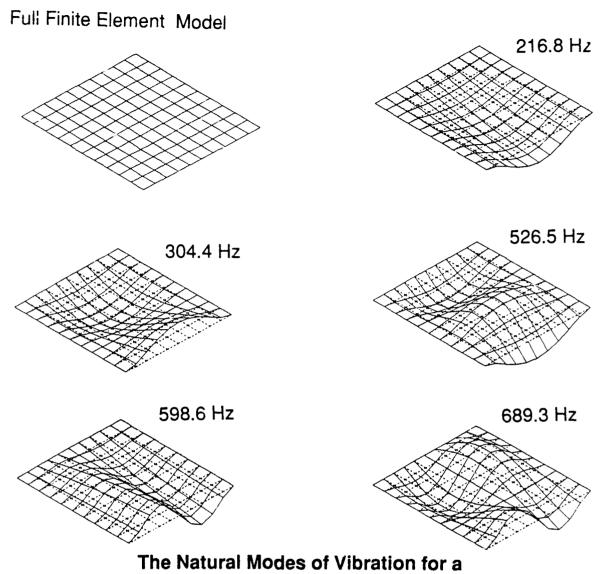


Figure 4–19. Half Model Finite Element Model Resonant Modes

the most damage to the components and can be predicted with only the symmetric boundary condition. Note that only symmetry to the stiffness matrix is assumed. When making refined PCB models which include the component mass, the finite element mass matrix may no longer be symmetric and will cause errors in the frequency prediction.

As an example, the natural modes of vibration in a half symmetric PCB model are shown in Figure 4–19. The frequencies and modes shown are for both the symmetric and antisymmetric boundary conditions. These are in complete agreement with the frequencies and modes extracted in the full model analysis shown in Figure 4–20.



Clamped-Clamped-Pinned-Free Plate

Figure 4-20. Full Finite Element Model Resonant Modes

To accurately predict stresses in lead geometries from a dynamic model of the PCB, it is necessary to model the components individually. Detailed solid-type finite elements are used throughout the board, ceramic case, and leads to account for the small lead geometries (Figure 4-21). This requires extensive modeling and an exorbitant number of degrees of freedom. To reduce the size of the finite element model, simplified models can be assumed using plate-type elements for the chip carrier and beam-type elements

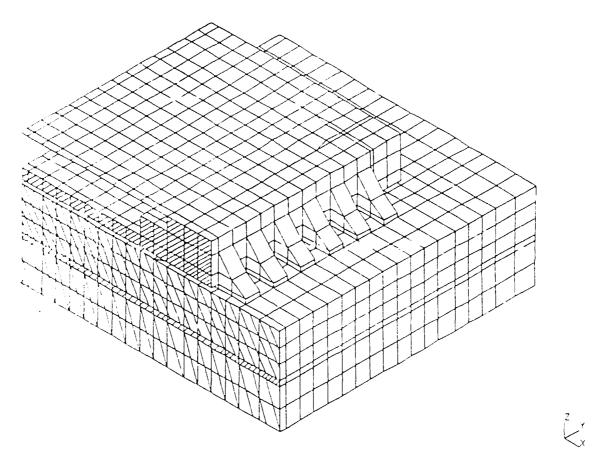


Figure 4-21. Small Lead Geometries

for the copper leads as described by Soovere et. al, (Ref. 4–5). The modeling described lumps groups of four to five of the side leads into a single beam placed at the center of the group pin location (Figure 4–22). The corner leads, which are the most critical, are individually modeled. The loads predicted by finde element analysis in the beam elements can then be applied to material failure models.

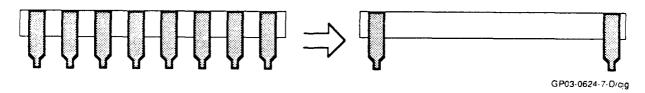
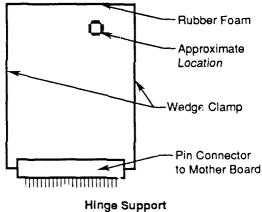


Figure 4-22. Lead Grouping

## Transferring Vibration Loads and Displacements onto Detailed Finite **Element Model of Component Leads**

The following example demonstrates how loads from a PCB level analysis are tensferred to a detailed lead analysis. The PCB configuration is depicted in Figure 4-23. The out-of-plane displacements due to random vibration were determined from a previous analysis to be 6.0028 inches rms at the chip center, Figure 4-24. Loads and displacements in the leads were found using the three-dimensional PCB/chip model in Figure 4-25. It consists of a PCB and chip carrier modeled with plate-type elements and leads individually modeled with bar-type elements. The PCB is clamped on the sides. simply supported on the top and free on the bottom. The model was only used to predict deflections; hence, the meshing lacks the necessary refinement to accurately predict stresses. The deflections in the lead wires, extensional and rotational, were determined for an applied displacement of 0.0028 inches at the chip center.



#### Chip

- Dimensions: 0.95 in. x 0.95 in, x 0.10 in.
- Material: Ceramic Weight: 0.007827 lb Description: 68 Lead,

Chip Carrier

- CTE: 6.4 ppm/deg C Modulus: 45E6 lb/in.\*\*2

#### **Board**

- Dimensions: 5.65 in. x 6.14 in. x 0.064in.
- · Material: Sandwich of Poly/Glass and Copper
- Weight: 0.327 lb
- Copper
- Modulus: 16.0E6 lb/in\*\*2
- $-\mu$ : 0.34
- · Poly/Glass
- Modulus: 2.0E6 lb/in\*\*2
- $-\mu$ : 0.34
  - GP03-0624-10-D/ks

Figure 4-23. PCB Configuration

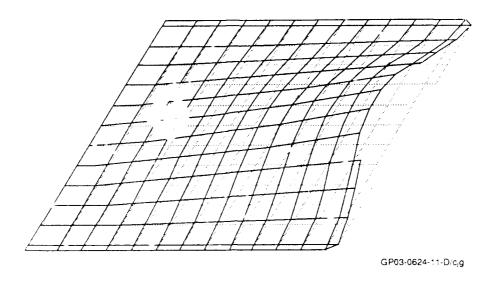


Figure 4-24. Out-of-Plane Displacements

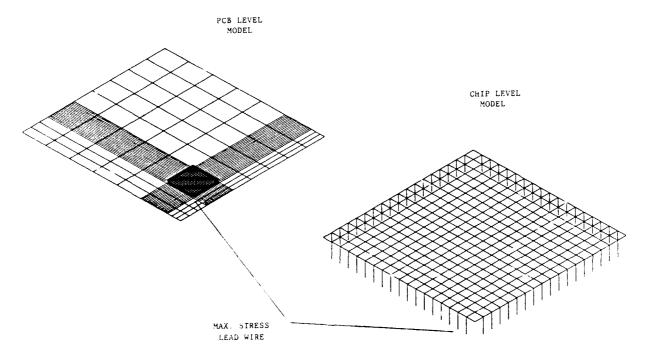


Figure 4-25. Three Dimensional FEA Model

For this detailed PCB level analysis, the leads were crudely modeled with bending bartype elements which have an approximate equivalent stiffness (k<sub>eq</sub>) to the J-lead depicted in Figure 4-26. Typically, properties of finite element bar elements include elastic modulus (E), width (W), thickness (Th) and length (L). The axial stiffness is given by Eq. 21.

$$K_{eq} (axial) = (E)*(W*Th)/(L)$$
 Eq. 21

The equivalent axial stiffness of the J-lead shown in Figure 4-26 is given by Eq. 22,

$$K_{eq} \text{ (axial)} = [(1/K_1) + (1/K_2) + (1/K_3)]^{-1}$$
 Eq. 22

where:

$$K_1 = 3E_1I_1/(L_1)^3$$
  
 $K_2 = E_1A_2/L_2$ 

$$K_3 = E_s A_s / L_s$$

Therefore, the elastic modulus used in the three dimensional lead elements was determined from Eq. 23,

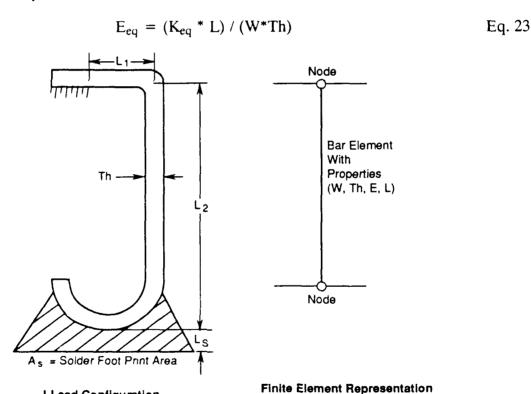


Figure 4-26. J-Lead Axial Stiffness Representation

In PCB Level Analysis

J-Load Configuration

GP03-0624-12-D/suz

From the three dimensional FEA, axial and bending loads were predicted for the leads. The maximum loads predicted were in the corner lead in the lower left hand side. This is due to the relative displacement of the chip with respect to the PCB as shown in Figure 4–27. These loads were then imposed as enforced displacements on a detailed three dimensional finite element model of the J-lead (Figure 4–28). The axial displacement and moment displacement were determined from Eqs. 24 and 25 respectively,

$$F_{axial}/K_{eq} = Axial Displacement (y_{axial})$$
 Eq. 24

$$XTan\theta$$
 = Bending Moment Displacement ( $y_{bending}$ ) Eq. 25

where: 
$$\theta = M^*L/(2EI)$$
 Eq. 26

and are shown in Figure 4-29.

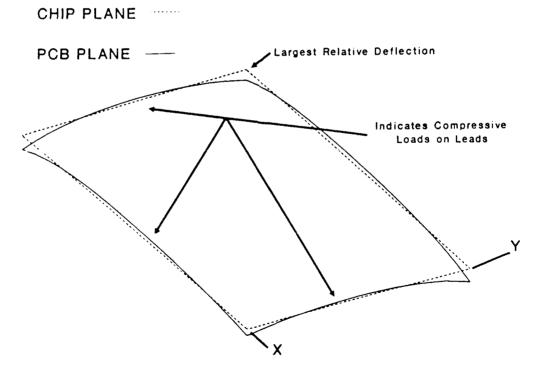


Figure 4-27. Relative Displacement - Chip to PCB

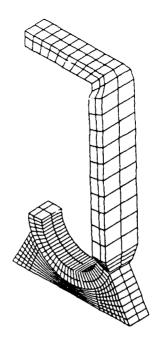


Figure 4-28. Detailed Three-Dimensional J-Lead FEM

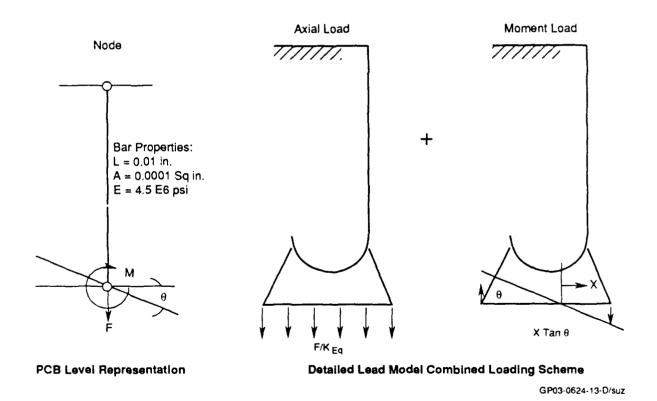


Figure 4-29. Axial and Moment Displacement

The results of the load transfer analysis are shown in Figures 4-30, 4-31, and 4-32. The deformation is illustrated in Figure 4-30. The peak load stress is 15,700 psi in the top horizontal arm of the lead shown in Figure 4-31. The peak solder stress is 1095 psi at the lead/solder interface shown in Figure 4-32.

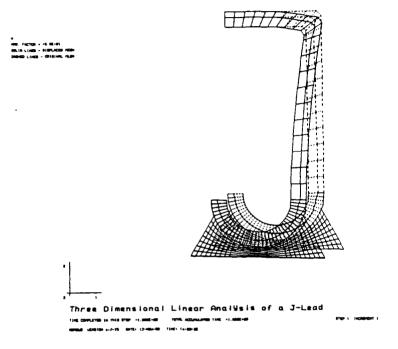


Figure 4-30. Load Transfer Analysis Results - Deformation

															1	
15785.	13711.	11716.	9722.	7723.	5733.	3739.	1745.	-249.	-2244.	-4238.	-6232.	-8227.	-18221.	-,2215.	-14210.	

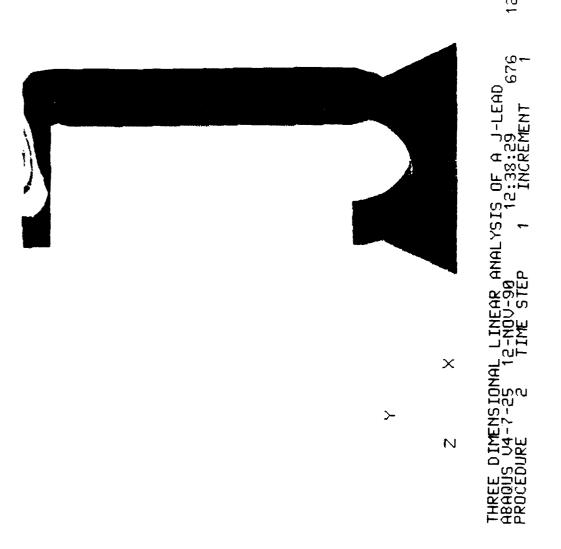
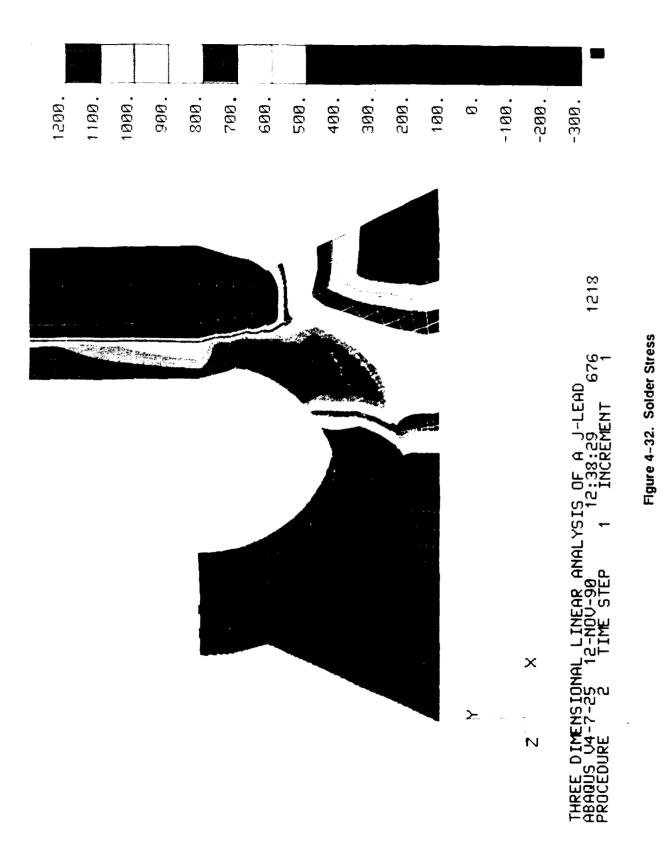


Figure 4-31. J-Lead Stresses



# 4.7 Modeling Consideration for Leads and Solder Joints

Several modelling and analysis techniques have been used to predict solder joint stresses (References 4-6, 4-7, 4-8, 4-9, 4-10 & 4-11). Modelling techniques employing both two and three dimensional assumptions have been demonstrated. Two dimensional models require a plane stress assumption in the state of stresses in the lead. The various three dimensional modelling techniques in the literature include partial models of the chip carrier, lead, so der joint and PCB. The chip carrier and PCB will be represented based on the type of component connections (surface mounted or poke thru). The following discussion will focus on modelling techniques which illustrate the failure mechanisms of components with leads and without. The examples will include rationale and explanation for any modelling assumptions.

# 4.7.1 Plated Through Hold (PTH) Lead and Solder Joint Failures

PTH failures normally occur during thermal cycling environments where expansion of the PCB in the Z-axis produces high tensile forces and stresses in the copper barrel of the PTH as shown in Figure 4-33. The PCB expands more than the copper in the PTH since the coefficient of thermal expansion (CTE) of the PCB is much higher than the CTE of the copper. When the number of stress cycles and the corresponding stress levels are high enough, a fatigue fracture can occur in the copper barrel and produce an electrical malfunction.

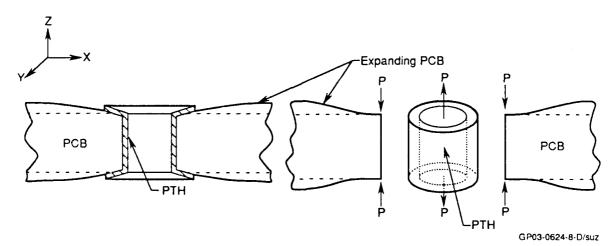
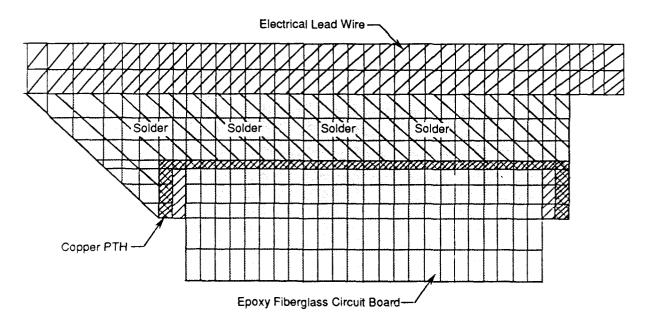


Figure 4-33. Plated Thru Hole Z-Axis Expansion

Two different FEM techniques can be used to determine the thermal expansion stresses induced in the structural elements; two dimensional (2–D) and three dimensional (3–D) modelling. Two dimensional modelling can be accomplished using plate-type elements where only the thermal expansion forces are acting; no external forces are acting on the electrical leads. It is necessary to model a segment of the connection including the lead, solder joint, copper barrel, and PCB (Figure 4–34). The differences in the CTE of the materials will generate the internal stress field. Three dimensional models must be constructed with isoparametric (solid) elements to obtain the full 3–D characteristics. Generally, the 3–D model represents the actual structure more accurately.

Most FEM codes have an eight node isoparametric element and a twenty node isoparametric element available. The eight node solid contains a linear stress distribution within the element. Therefore, when the stress distribution through a structure is known to be linear, the use of the eight node element will save a considerable amount of computer time because there are far fewer node points in the model.



GP03-0624-9-D/gms

Figure 4-34. Plated Through Hole Section

When the boundary conditions are properly defined, it is often easier to slice a section out of the 3-D model, as shown in the Figure 4-35. To simplify the model by reducing the number of solid elements, a 30° slice is removed from the fall model. This section examines the stress distribution in the 30° slice (cyclic symmetry has been assumed).

A relatively simple model can be constructed if the magnitude of the external lead loads are known from prior experiments. Very often the magnitude of the external loads are not known, so the model developed must include the structural elements responsible for producing the critical loads.

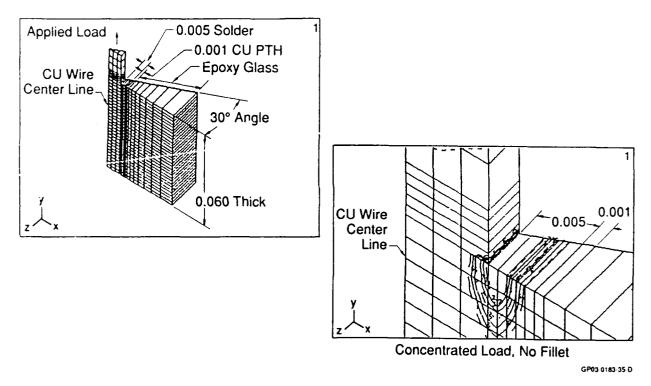


Figure 4-35. Three Dimensional Model Slice

## 4.7.2 Thermal Expansion Stress Analysis in DIPs

Another type of thermal expansion problem that can be solved using FEM techniques involves long components such as DIPs and hybrids. A typical quarter model of a DIP on a PCB is shown in Figure 4–36. The DIP component has a much lower CTE than the PCB in the x-y plane of the PCB. At the high temperature end of the thermal cycle, the

PCB expands more than the component. This produces relative bending in the electrical leads as shown in the schematic in Figure 4-37. In Section 4.8, examples show how the loads on the lead wires can be determined. Methods for modelling the electrical leads on the DIP are shown in Figure 4-38.

The leads generate a shear tearout stress in the PCB solder joint due to the bending moment induced by the relative expansion difference between the component and the PCB. The solder joint should not be allowed to exceed a true value of about 400 psi to insure a 15 to 20 year life in an environment where extensive thermal cycling is expected.

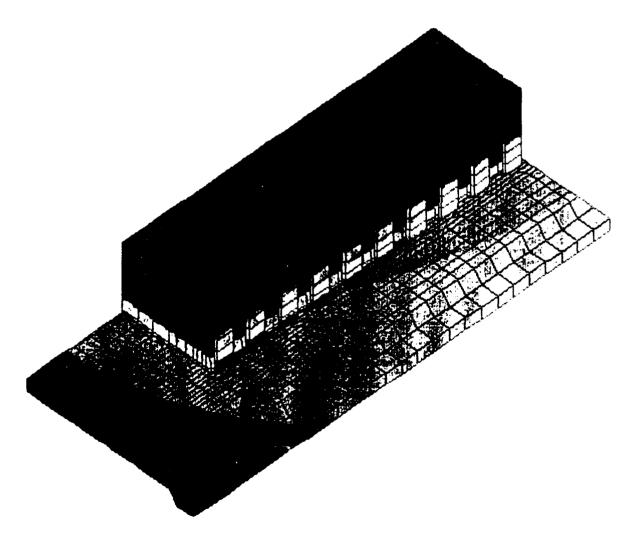


Figure 4-36. Quarter Model of DIP on PCB

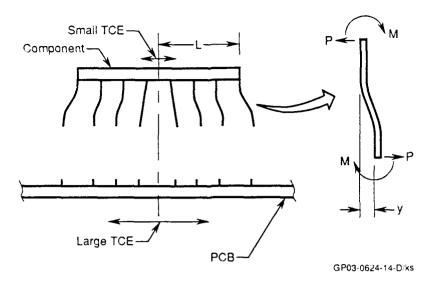


Figure 4-37. Thermal Expansion in Plane

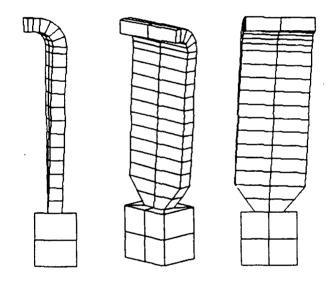


Figure 4-38. Modelling DIP Leads

Some typical methods for modelling the leads and solder joints for a DIP are shown in Figure 4–39. Many different combinations of isoparametric solid elements, shell elements and beam elements can be combined to develop the model.

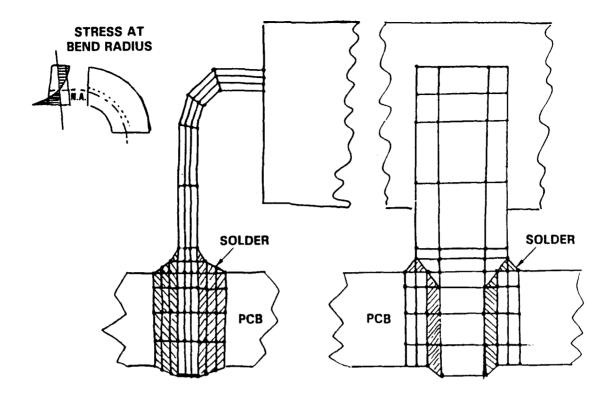


Figure 4-39. DIP Lead and Solder Model

# 4.7.3 Thermal Stress Analysis in LCCCs

Leadless ceramic chip carrier (LCCC) components are being used in great quantities for surface mount PCBs. The ability of these components to survive extended thermal cycling environments is determined by the solder joint that supports these devices. The solder point integrity is directly related to the solder joint fatigue properties and the quality of the process that manufactures the solder joints. Since the process controls are not a design function, the emphasis here is directed towards a better understanding of the creep characteristics and fatigue properties of the solder joints at various temperatures and thermal cycling conditions.

The most common solder used today is a eutectic solder with 63% tin and 37% lead and a melting point of about 184°C. Its tensile strength and its modulus of elasticity show an increase with an increase in the loading rate. These same factors show a decrease with increasing temperatures. The stress-strain curve is highly non-linear, as shown

in Figure 4-40, and its modulus of elasticity rapidly decreases with increasing temperature as shown in Figure 4-41. Solder is highly strain rate sensitive as shown in Figure 4-42.

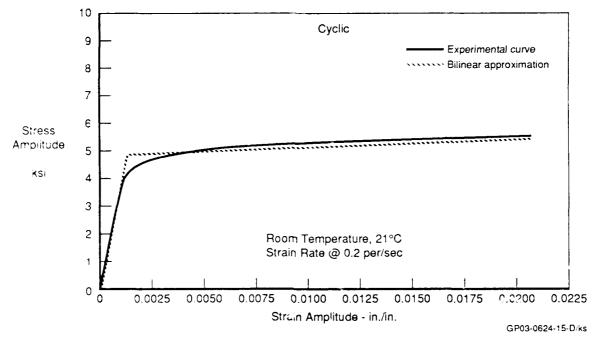


Figure 4-40. Highly Nonlinear Stress-Strain Curve

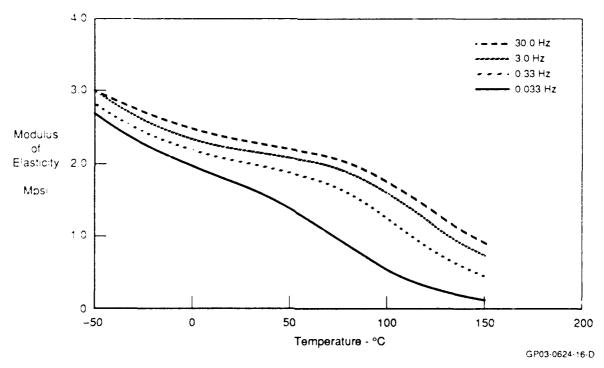


Figure 4-41. Modulus Change With Temperature

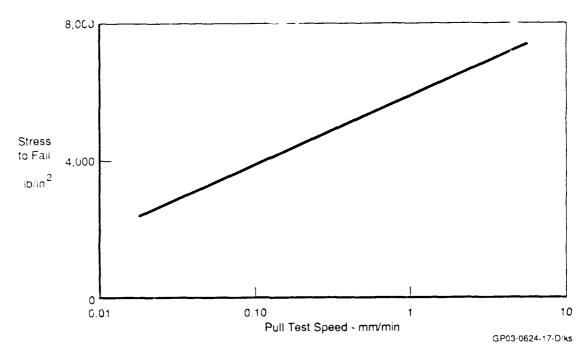


Figure 4-42. Strength vs. Strain Rate

It tends to exhibit stress relaxation at high temperatures, above 100°C. Solder will also rupture from creep under the action of a steady applied load for extended periods, as shown in Figure 4–43. Another unusual characteristics of eutectic solder is that its stress fatigue life is directly related to frequency of the alternating load as well as the temperatures, as shown in Figure 4–44.

Section 4.8 will illustrate typical models used for LCCC devices and leaded surface mount components.

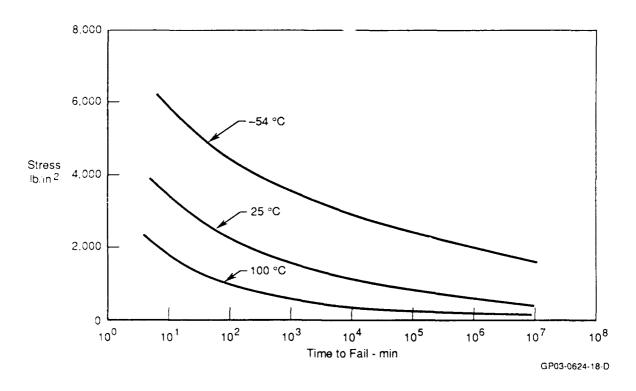


Figure 4-43. Constant Load vs. Life for Solder (Creep)

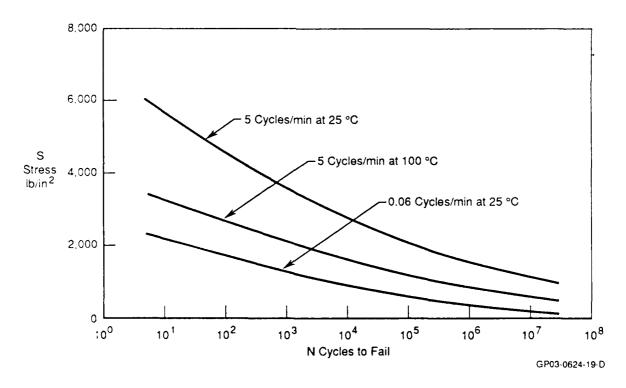


Figure 4-44. Fatigue Life vs. Cycle Rate and Temperature

## 4.8 Thermal Stress Solder Joint Finite Element Analysis

This section describes thermal stress analyses of a J-lead solder joint and a leadless chip carrier solder joint. The J-lead problem was analyzed using five different procedures. The first and second procedures consist of a two dimensional (2-D) Nastran and a 2-D ABAQUS analysis. The third procedure used a similar 2-D Probe analysis. The fourth procedure consists of a 2-D Probe analysis of the joint and the chip carrier, and finally, the fifth procedure consists of a 2-D Probe analysis of the joint, the chip carrier and the PCB. The fifth part examines the effect of allowing thermal expansion in both the vertical and horizontal directions.

The second example is a linear elastic finite element analysis (FEA) of a leadless solder joint and compares four different procedures. The first procedure used a 2-D ABAQUS model of the solder joint subjected to thermal displacements. The second approach consists of a 2-D Probe analysis of the solder material. The third approach consists of a 2-D Probe analysis of the solder joint and the chip carrier. The fouth part consists of a 2-D Probe analysis with the chip carrier and an applied temperature differential, which examines the effect of allowing thermal expansion in both the horizontal and vertical directions.

These examples address the accuracy of the stress/strain analysis of the lead/solder joint. Nastran and ABAQUS are h-version finite element codes. Probe is a p-version finite element code from the MacNeal-Schwendler Corporation. In Nastran and ABAQUS, the discretization error is controlled by mesh refinement. In Probe, the discretization error is controlled by increasing the polynomial degree of the interpolation function and/or mesh refinement (Figure 4-45). When using Probe, the relative error in energy can easily be established by performing successive analysis at three different p-levels. Calculating the relative error in the strain energy and monitoring the convergence of functionals across like element boundaries ensures the quality of the finite element analysis. The functionals include stresses, strains, and stress resultants.

An additional quality control benefit of using p-version technology is the minimization of round-off error, of concern because of the very small elements used to model the joints. These quality control procedures are integral to extracting the location and magnitude of stresses/strains for use in fatigue life predictions.

#### WHAT IS MEANT BY P-VERSION AND H-VERSION

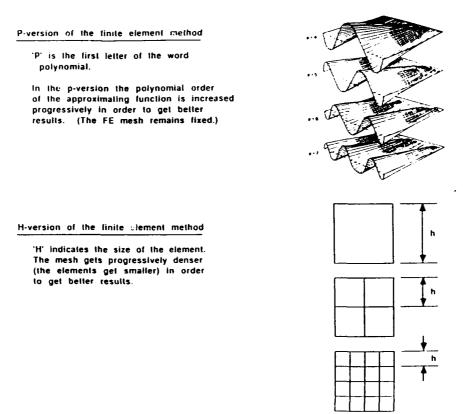


Figure 4-45. Discretization Error Control

## 4.8.1 J-lead/Solder Joint Finite Element Model Geometry

The 2-D plane stress finite element models (FEM) of the J-lead/solder joint are shown in Figures 4-46 and 4-47. The basic J-lead/solder FEM consists of the following:

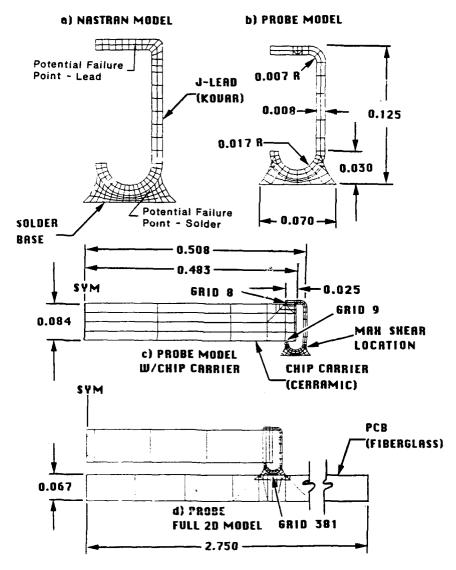


Figure 4-46. J-Lead / Solder Joint Geometry

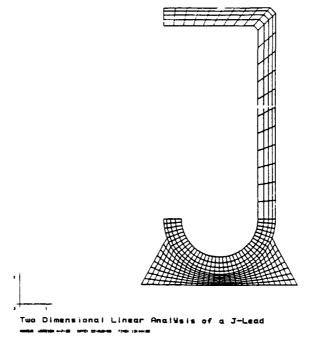


Figure 4-47. ABAQUS FEM

- 1) The Kovar J-lead material is 0.008 inches thick.
- 2) The height of the J-lead/solder joint is 0.125 inches.
- 3) The chip carrier is 0.084 inches thick.
- 4) The PCB is 0.067 inches thick.
- 5) All finite element models have a membrane thickness of 0.012 inches for the plane stress analysis.
- 6) Material properties for the various materials used in the J-lead/solder joint are shown in Table 4-3.
- 7) The 60Sn/40Pb solder material properties are at room temperature conditions.
- 8) Symmetric boundary conditions are used so that only one half of the chip carrier and PCB are modeled.

**TABLE 4-3. MATERIAL PROPERTIES** 

Material	Elastic Modulus (psi)	Poisson's Ratio	Thermal Expansion (in/in/deg C)		
Kovar	2.E+07	0.31	5.5E-06		
60/40 Solder	2.E + 06	0.40	28.0E-06		
Chip Carrier	54.E+06	0.25	6.4E-06		
PCB	2.E + 06	0.15	9.5E-06		

## 4.8.1.1 ABAQUS & Nastran Finite Element Analysis of the J-lead/Solder

The Nastran FEM is shown in Figure 4-46a and consists of 78 Quad4 membrane lead elements and 56 Quad4 membrane solder elements. The ABAQUS FEM is shown in Figure 4-47 and consists of 228 lead elements and 216 solder elements.

The top flange of the J-lead in both models is fixed in both the X (horizontal) and Y (vertical) directions. The applied loading represents the differential thermal expansion in the plus X direction, between the chip carrier and PCB, due to a power up cycle. This plus X expansion will be called the PXTHERM load condition. The temperature differential ( $\Delta T = T_{max} - T_{min}$ ) of the chip carrier was assumed to be 53 degrees C and the temperature differential of the PCB was assumed to be 46 degrees C for the power up cycle. The loading was applied to the FEM using imposed displacements in the X direction along the base of the solder as shown in Figure 4–48a. At the left corner of the solder base the imposed displacement is  $\pm .319E-04$  inches in the X direction. At the right corner of the solder base the imposed displacement is  $\pm .625E-04$  inches in the X direction. These displacements were calculated using the following formula:

$$\Delta x = C1 * (x + C4) - C2 * C3.$$
 Eq. 27

where: C1 = 4.37E-4 in/in, PCB thermal strain

C2 = 3.392E-4 in/in, chip thermal strain

C3 = .483 in., one half the chip length

C4 = .448 in., center of the chip to beginning of solder

The entire length of the solder base was restricted from any motion in the Y direction.

The resultant stresses at potential failure points (Figure 4-46a) are shown in Table 4-4. The stress on the inner surface of the upper J-lead elbow was extrapolated from stresses provided at the element centers. As shown in Figure 4-46a, only a crude representation of the elbow was made in the Nastran FEM. This is the reason for the low stresses calculated in this region of the Nastran FEM. Stress contours for the Nastran FEA are shown in Figure 4-49 and the deflected shape is shown in Figure 4-48a. Similar results were

obtained with ABAQUS. The displacements were scaled by a factor of 1000 to clearly show the deformations. A graphical representation of the boundary conditions is included. An important characteristic of the deformed shape is the elongation of the J-lead and solder base.

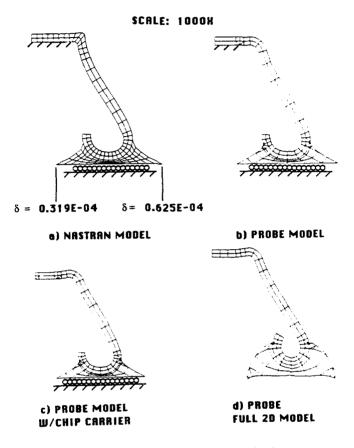
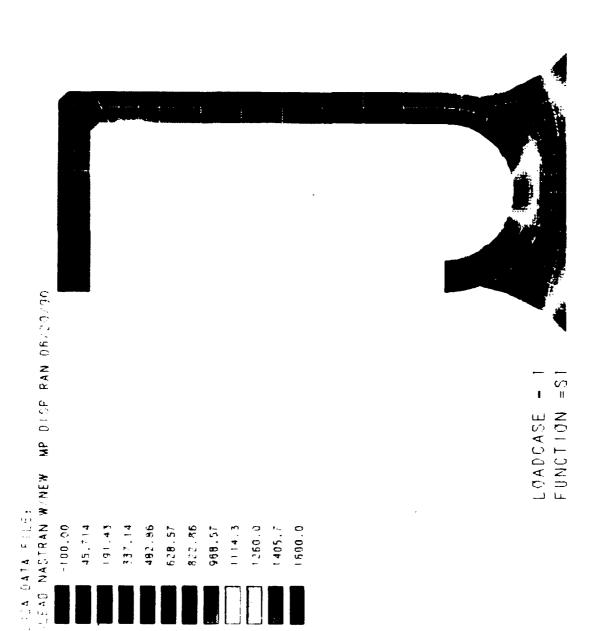


Figure 4-48. Loading and Imposed Displacements



44

Figure 4-49. (a) Max Principal Stress - Nastran FEA

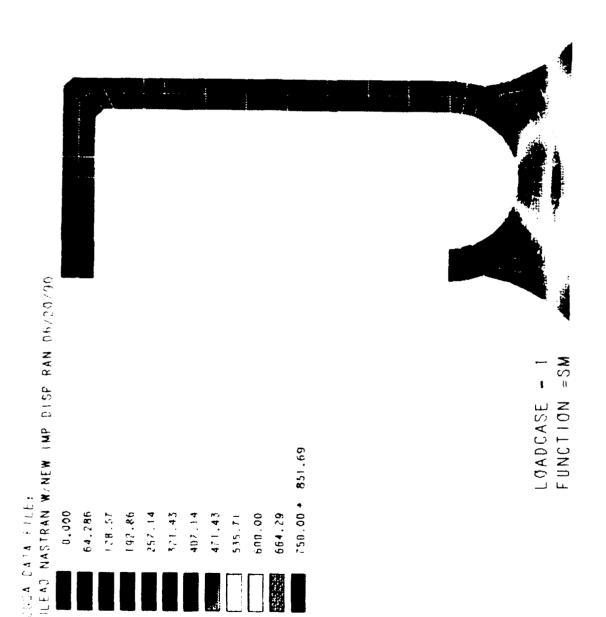


Figure 4-49. (b) Max Shear Stress - Nastran FEA

TABLE 4-4. J-LEAD SOLDER JOINT STRESSES/STRAINS

FEM C	ode Model	Load Condition	Principal Stress Lead Elbow (psi)	Max. Shear Stress Solder (psi)
ABAQUS	J-Lead/Solder Section 4.8.1.1	PXTHERM: Imposed Displacements to Simulate Chip Carrier/ Board Expansion	2580	98
NASTRAN	J-Lead/Solder Section 4.8.1.1	PXTHERM: Imposed Displacements to Simulate Chip Carrier/ Board Expansion	750	90
PROBE	J-Lead/Solder Section 4.8.1.2	PXTHERM: Imposed Displacements to Simulate Chip Carrier/ Board Expansion	1840	94
PROBE	J-Lead/Solder W/Chip Carrier Section 4.8.1.3	PXTHERM: Imposed Displacements to Simulate Chip Carrier/ Board Expansion	1390	43
PROBE	J-Lead/Solder W/Chip Carrier Section 4.8.1.3	PDTEMP: Applied Temperature & PXTHERM: Imposed Displacements to Simulate Chip Carrier/ Board Expansion	1240	1260
PROBE	Full 2-D Model (J-Lead/Solder W/Chip Carrier & PC Board) Section 4.8.1.4	PDTEMP: Applied Temperature	1400	1240

## 4.8.1.2 J-Lead/Solder Joint Probe Finite Element Analysis

Figures 4–46b through 4–46d are Probe FEM'S used to investigate the effects of using different boundary conditions and load conditions within the J-lead and solder joint finite element analyses. The FEM in Figure 4–46b was analyzed using the identical boundary conditions and load conditions as the Nastran FEM shown in Figure 4–46a. It contains 76 J-lead elements and 31 solder elements. A comparison of the stress results presented in Table 4–4 shows higher stresses calculated with Probe, using a p-level of 8, than those calculated using NASTRAN. The Nastran analysis used linear interpolation within the element boundaries, which is equivalent to a p-level of 1. The stresses in Table 4–4 are located at potential crack initiation points, shown in Figure 4–46.

The Probe FEM included mesh refinements around the area of the J-lead and solder intersections. This was necessary to ensure convergence of both energy and stresses/ strains in the area of interest. In general, a finite element analysis ensures only displacement continuity across element boundaries. The Probe FEA used higher order interpolation functions and mesh refinement to ensure that the stresses/strains converged across like element boundaries within some acceptable tolerance. In the Probe analysis, the tolerance was less than 3% in stresses across J-lead element boundaries and solder element boundaries. The stresses across J-lead element and solder element boundaries will always be discontinuous because of the differences in material properties at the interface. Stress contours for the Probe FEA are shown in Figure 4-50.

The Nastran FEA provides stresses at element centers. In Nastran, stresses calculated at the same grid point from different elements will not be the same. When grid point stresses are calculated in Nastran, a weighting procedure is used which gives an average stress at the grid point. The grid point stress averaging procedure can produce misleading results near the J-lead/solder material interface if separate averaging procedures are not used for the different materials. A single stress averaging process across different material

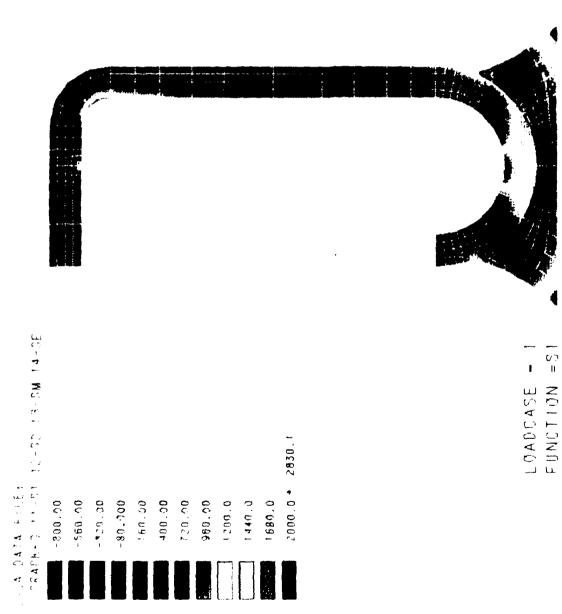


Figure 4-50. (a) Max Principal Stress - Probe FEA

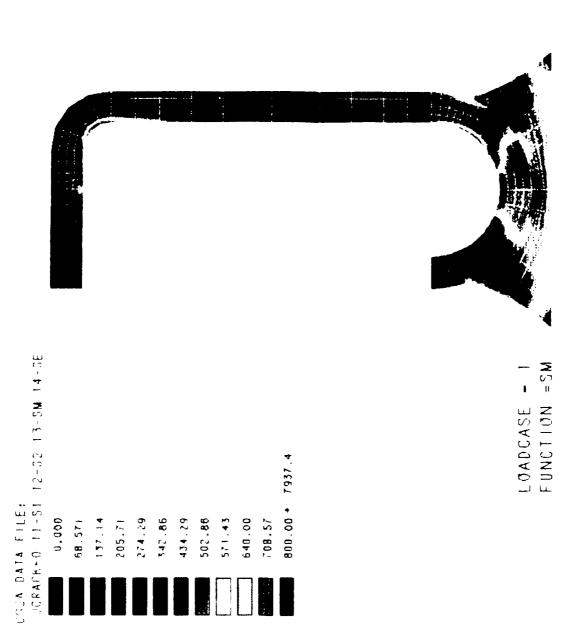


Figure 4-50. (b) Max Shear Stress - Probe FEA

boundaries will generate a single value at the grid point using an average of stresses on either side of the material interface. Other finite element codes use similar methods to extract grid point stress results. The methods of extracting grid point stresses is important and is one of the reasons for the discrepancies between the Nastran FEA and the Probe FEA.

The deflected shape of the Probe FEM is shown in Figure 4-48b. Included is a graphical representation of the boundary conditions, identical to the Nastran FEM of Figure 4-48a. The deformed shape is very similar to the deflected shape of the Nastran FEM of Figure 4-48a. Again, the J-lead and solder base elongation is noticeable.

#### 4.8.1.3 J-lead/Solder Joint Probe FEA with Chip Carrier

The Probe FEM in Figure 4-46c is similar to the Probe FEM in Figure 4-46b except for the addition of the symmetric portion of the chip carrier. This model includes 83 Jlead finite elements, 31 solder finite elements and 60 chip finite elements. Only half of the chip carrier is modeled because of symmetry. The addition of the chip carrier allowed symmetrical boundary conditions to be used with the model. The symmetrical conditions assume all motion in the X and Y direction is fixed at the center of the chip carrier. In the previous Nastran and Probe analyses, all motion in the Y direction was fixed at the upper flange of the J-lead. Two load conditions were applied to this 2-D Probe FEM. The first load condition (PXTHERM) was identical to that used in the previous Nastran and Probe analysis. The second load condition (PDTEMP) included the thermal expansion induced load between the J-lead material and solder material. Load condition 1 and 2 represent the thermal expansion mismatch between the chip carrier and PCB in the plus X direction. The applied temperature differential ( $\Delta T = T_{max} - T_{min}$ ) for load condition 2 (PDTEMP) was 50 degrees C. The temperature differential in this case effected only the J-lead and solder materials. The thermal expansion of the chip carrier and PCB were included in the PXTHERM imposed displacements. Therefore, the CTE of the chip carrier was set equal to 0.0 when the second load condition was applied.

The differences between the results of the Probe FEA of Section 4.8.1.2 and this Probe FEA for the PXTHERM load condition are a direct result of the relaxation of the Y direction support of the upper J-lead flange. Removing the Y direction support allowed the chip carrier to move down towards the PCB when the load was applied. As shown in Table 4-4, the J-lead upper elbow stress was reduced from 1840 psi to 1390 psi when the Y direction support was eliminated. This is also noticeable in stress contours around the upper flange radius as shown in Figure 4-50 and 4-51. The deflected shape for the PXTHERM load condition is shown in Figure 4-48c. Graphical representation of the boundary condition at the base of the solder is included. Again, there is elongation of the solder base. There is a slight change in the deformed shape of the upper J-lead flange attributed to the relaxation of the Y direction support. The deflected shape for the second load condition is similar to that shown in Figure 4-48d with the exception of the flat solder base.

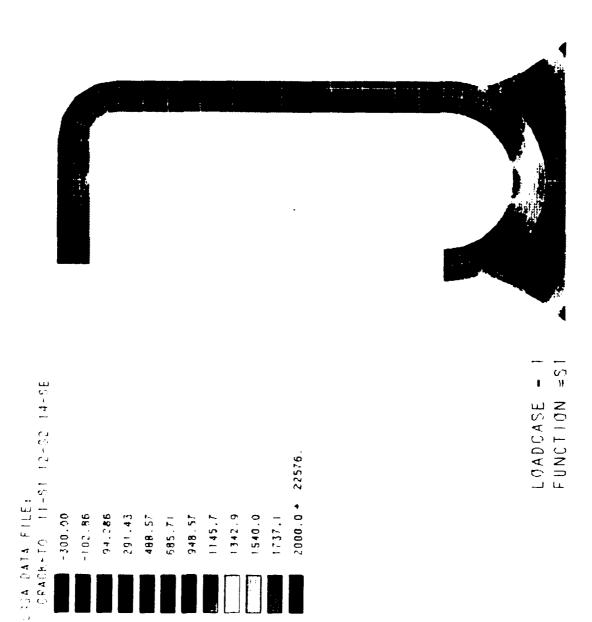


Figure 4-51. (a) Max Principal Stress - Probe w/Chip FEA

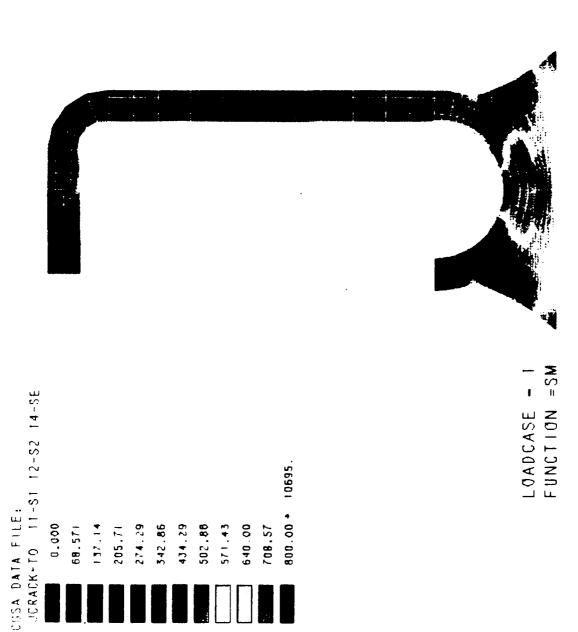


Figure 4-51. (b) Max Shear Stress - Probe w/Chip FEA

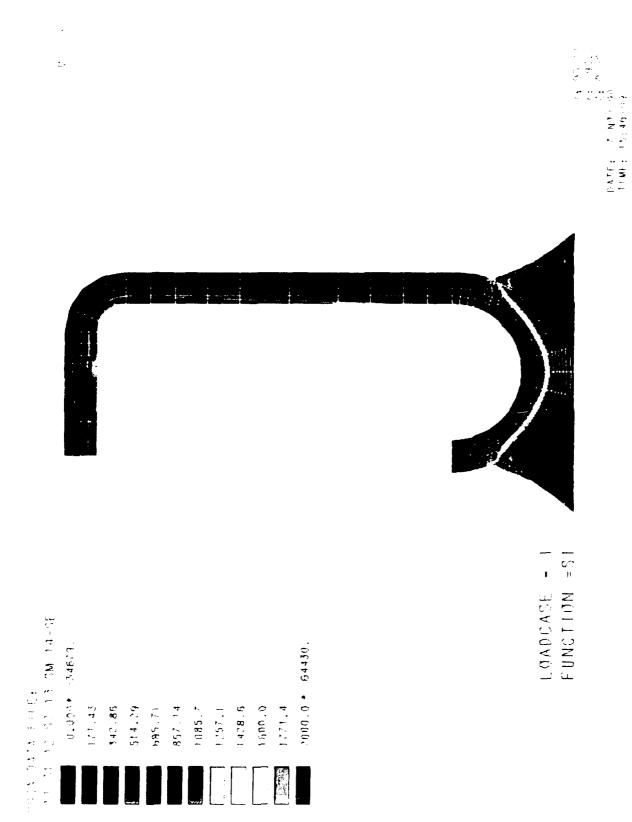
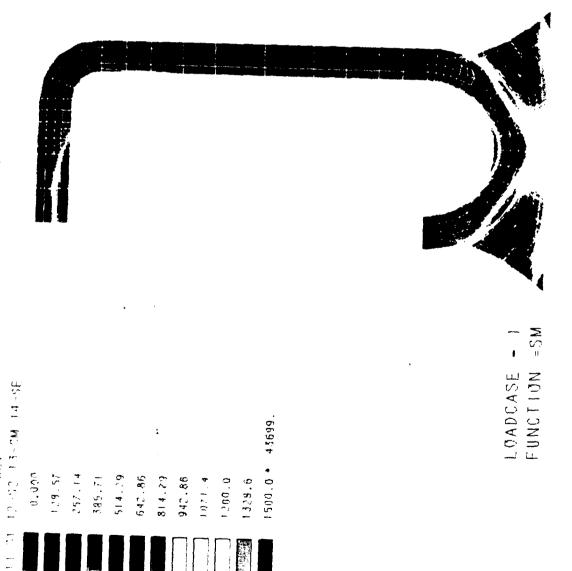


Figure 4-51. (c) Max Principal Stress - Probe w/Chip FEA



4 96 55 1 96.5 7: 96.5 7: 0.00 1146: 15:56:27 Figure 4-51. (d) Max Shear Stress - Probe w/Chip FEA

1500.0





EGADCASE - 1 FUNCTION =SI

9.000 000E-3 500E-3

2 000E-3 +3,452E-3

10x 0x1x 0x1E; 10x10x10x20x10xEM 14xEE

0\_000 + 1\_790E-4

2 000E-4 4 000E-4 5 000E-4 9 000E-4 000E-3

5-96-3

7378-3

658E - 3

1 815E-3 1 895E-3

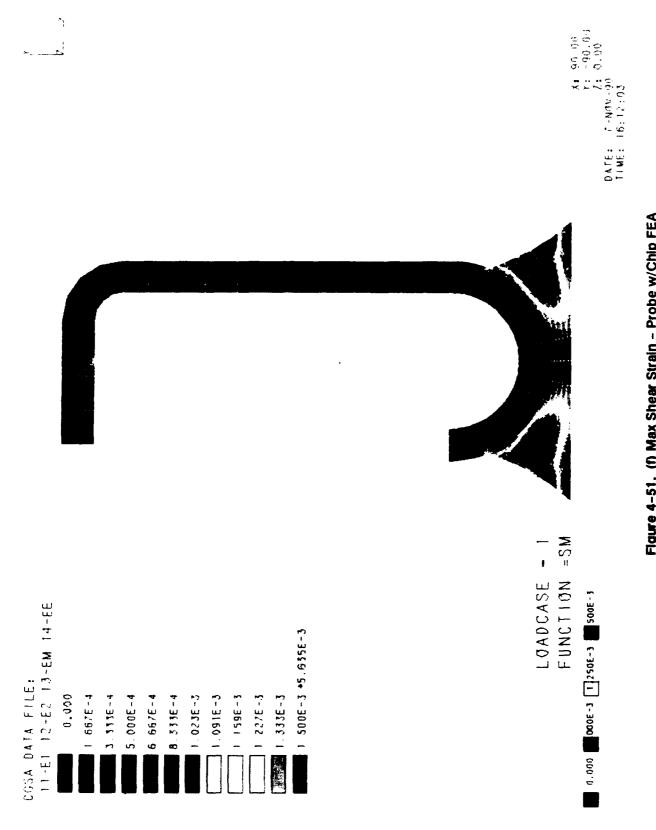


Figure 4-51. (f) Max Shear Strain - Probe w/Chip FEA

#### 4.8.1.4 J-lead/Solder Joint Probe FEA, Full 2-D Model

The Probe FEM in Figure 4-46d includes the J-lead/solder joint, the chip carrier and the PCB. This model contains 68 J-lead elements, 37 solder elements, 13 chip carrier elements, and 76 PCB elements. Symmetrical conditions are imposed at the center of the chip carrier and at the center of the PCB. Only one half of the chip carrier and PCB are modeled because of symmetry. Motion in the X direction is fixed and motion in the Y direction is free along the line of symmetry and the right edge of the PCB was constrained in the y direction. The applied temperature differential is 50 degrees C and will be called the PDTEMP load condition. Previous finite element analyses considered the differential expansion between the chip carrier and PCB in the plus X direction only.

The results in Table 4–4 show a big difference in the maximum shear stress between the FEA using the PDTEMP load conditions and the FEA using the PXTHERM load conditions. The stress contours of Figure 4–52 shows the concentration of stress around the area where cracks are known to propagate. This indicates the importance of including the differential expansion between all materials and the use of realistic boundary conditions. These results compare well with the second load condition of the Probe model in section 4.8.1.3, although the maximum shear strain for the Probe FEM of section 4.8.1.3 was slightly higher because the solder base remained flat. The increase in the J-lead elbow stress from 1240 psi to 1400 psi was due to the increased deflections of the PCB.

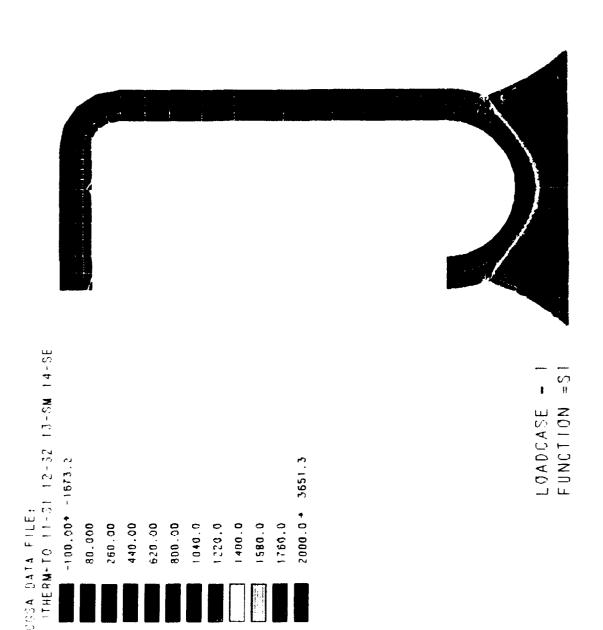


Figure 4.52. (a) Max Principal Stress - Probe w/Thermal Loads

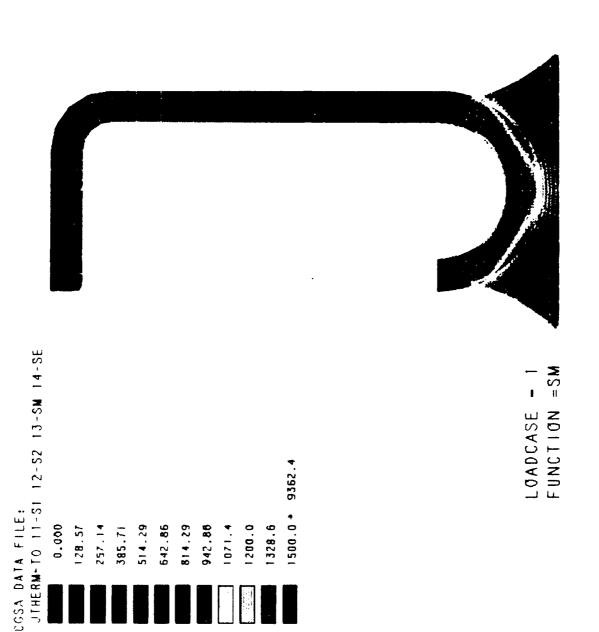


Figure 4-52. (b) Max Shear Stress - Probe w/Thermal Loads

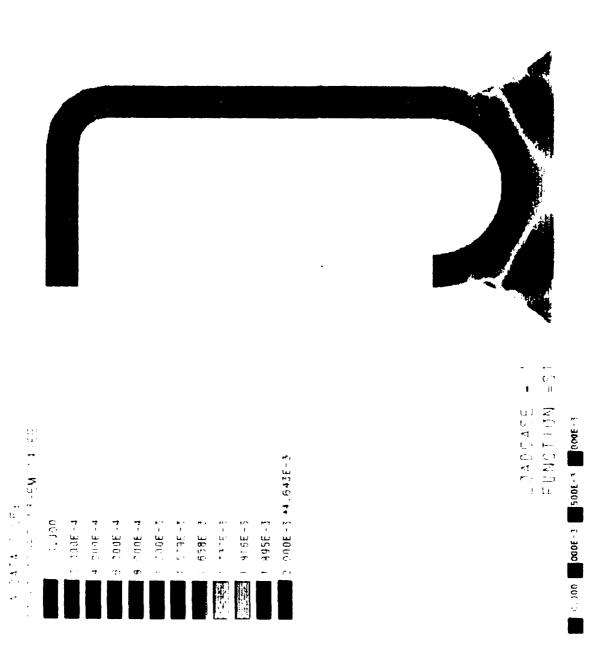


Figure 4-52. (c) Max Principal Strain - Probe w/Thermal Loads

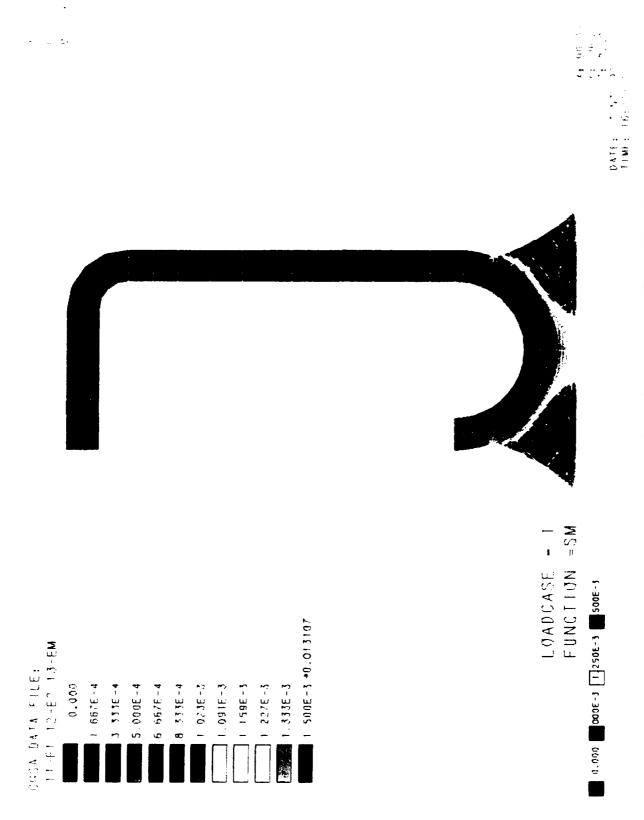


Figure 4-52. (d) Max Shear Strain - Probe w/Thermal Loads

The deflected shape is shown in Figure 4-48d. There is a clear difference between the deformed shape of this Probe FEM and the other FEMs shown in Figures 4-48 a through c. The deformations at the J-lead/solder boundary result from the thermal expansion coefficients mismatch. The displacements at the center of the solder base and at the upper J-lead flange/chip carrier interface are listed in Table 4-5. These grid locations are shown in Figure 4-46. The displacements in the X direction match up well with the expected thermal expansion at 50 deg C. The displacements at the center of the solder base are larger than those used in the previous analysis because of the larger temperature differential applied to the PCB. The previous analysis assumed a 53 degree C temperature differential within the chip carrier and a 45 degree C temperature differential within the PCB. The 50 degree C temperature represented an average of these two temperatures.

TABLE 4-5. THERMAL DISPLACEMENTS

Grid	x	Υ	<u></u> δ <b>X</b>	<u>8</u> Y	Calculated $(\delta T = 50 C)$ $\delta X = \delta * T * L$	Error %
8	0.10CE-01	0.117E+00	0.14^^=-03	0.2842E-03	0.1466E-03	0.00
9	0.100E-01	0.121E + 00	0.146∪~-03	0.2854E-03	0.1466E-03	0.00
381	0.350E-01	0.000E + 00	0.2299E-03	0.2414E-03	0.2294E-03	0.21

#### 4.8.2 Leadless Solder Joint FEAs

The analyses of leadless solder joints with Probe FEMs was accomplished in three steps: one with the solder only; one with the solder and chip carrier; and one with the solder, chip carrier, PCB and temperature change. ABAQUS was used to model the solder joint only.

#### 4.8.2.1 Leadless Solder Joint Probe FEA

The leadless solder joint geometry is shown in Figure 4-53a and the material properties are shown in Table 4-3. This geometry was generated using information from Reference 4-6. The 2-D Probe FEM contains 90 solder elements. For boundary conditions at the vertical support, motion is fixed in the X direction and motion is free in the Y direction. For boundary conditions at the horizontal support, motion is fixed in the X direction and Y direction. The applied loading represents the differential thermal expansion

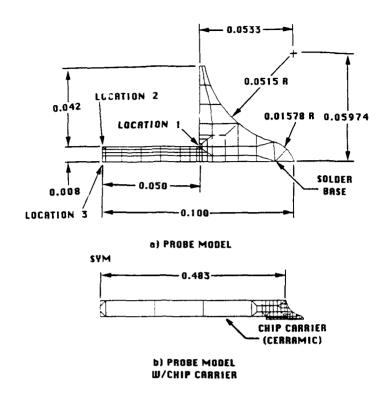


Figure 4-53. Leadless Soider Joint Geometry

in the plus X direction between the chip carrier and PCB. This plus X expansion is called the PXTHERM load condition. The temperature differential ( $\Delta T = Tmax - Tmin$ ) of the chip carrier is 53 degrees C and the temperature differential of the PCB is 46 degrees C. The loading was applied to the finite element model using imposed displacements in the plus X direction along the base of the solder as shown in Figure 4-54. At the left corner of the solder base, the imposed displacement is +.424E-04 inches in the X direction. At the right corner of the solder base, the imposed displacement is +.691E-04 inches in the X direction. These displacements were calculated using the following formula:

$$\delta x = (C1 - C3) * (x + C2), \text{ when } -0.05 < x < 0.00$$
 Eq. 28  
 $\delta x = C1 * (x + C2) - C3 * C2,$  when  
 $0.00 < x < 0.05$  Eq. 29

where: C1 = 4.37E-4 in/in, PCB thermal strain

C2 = .483 in, one half chip carrier length

C3 = 3.392E-4 in/in, chip carrier thermal strain

The entire length of the solder base was restricted from any motion in the Y direction.

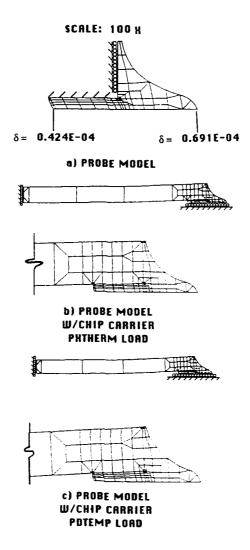


Figure 4-54. Loading and Imposed Displacements

The resultant stresses at potential failure locations (shown in Figure 4–53) are included in Table 4–6. As expected, the sharp notch near the chip carrier corner was the location of the peak stress although there were also high stresses at the left end of the solder joint. The stress contours for the 2–D Probe FEA are shown in Figure 4–55. The deformed shape shown in Figure 4–54a indicates shear deformation along the solder base between the chip carrier and PCB. The displacements were scaled by a factor of 100 to clearly show the deformations. A graphical representation of the boundary conditions used in the FEA is included.

# TABLE 4-6. LEADLESS CHIP CARRIER SOLDER JOINT

#### **Max. Shear Stress**

		Location 1:	Location 2:	Location 3:
Model	Load Condition	Near the Chip Carrier Corner (PSI)	Upper Left End (PSI)	Lower Left End (PSI)
Solder Joint Section 4.8.2.1	PXTHERM: Imposed Displacements to Simulate Chip Carrier /Board Expansion	11100	5970	2170
Solder Joint W/ Chip Carrier Section 4.8.2.2	PXTHERM: Imposed Displacements to Simulate Chip Carrier /Board Expansion	3120	1070	1590
Solder Joint W/ Chip Carrier Section 4.8.2.3	PDTEMP: Applied Temperature & PXTHERM: Imposed Displacements to Simulate Chip Carrier /Board Expansion	6100	2300	2460

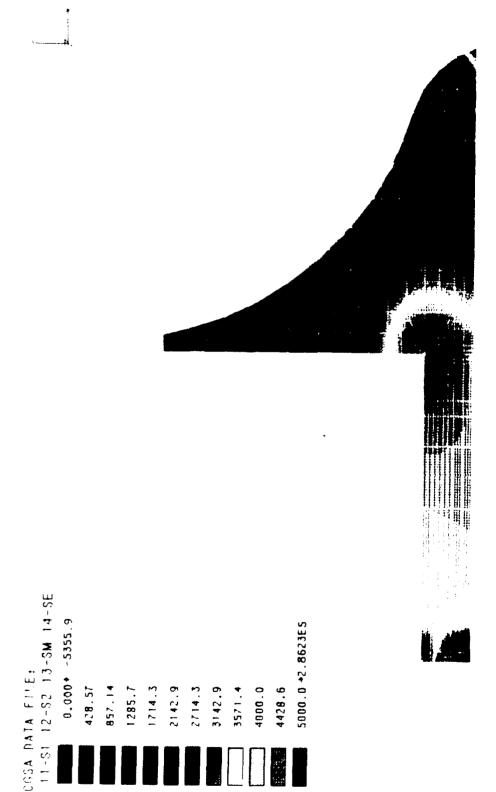


Figure 4-55. (a) Max Principal Stress - Probe FEA

4-101

= 5

LOADCASE .

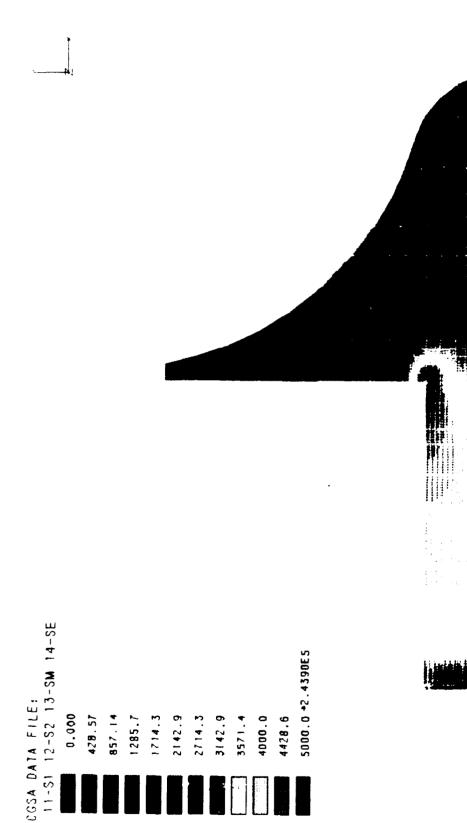


Figure 4-55. (b) Max Shear Stress - Probe FEA

LOADCASE - 1 FUNCTION =SM

# 4.8.2.2 Leadless Solder Joint Probe FEA with Chip Carrier

The leadless solder joint with chip carrier geometry is shown in Figure 4–53b and the material properties are shown in Table 4–3. The geometry was generated using information from Reference 4–6. The 2–D Probe FEM contains 97 solder elements and 64 chip carrier elements. Symmetric boundary conditions were used at the center of the chip carrier. Motion in the X direction is fixed and motion in the Y direction is free. At the solder base motion in the Y direction is fixed and motion in the X direction is free. The applied loading represents the differential thermal expansion in the plus X direction between the chip carrier and PCB and is identical to that used previously in section 4.8.2.1. This load condition is called PXTHERM.

The resultant stresses at potential failure locations are shown in Table 4-6. As expected, the sharp notch near the chip carrier corner was the location of the peak stress. When the chip carrier was added to the leadless solder joint FEM, the magnitude of the solder stresses decreased because of chip carrier bending. The stress contours for the 2-D Probe FEA are shown in Figure 4-56.



LOADCASE - 1 FUNCTION =S1

Figure 4-56. (a) Max Principal Stress - Probe w/Chip FEA

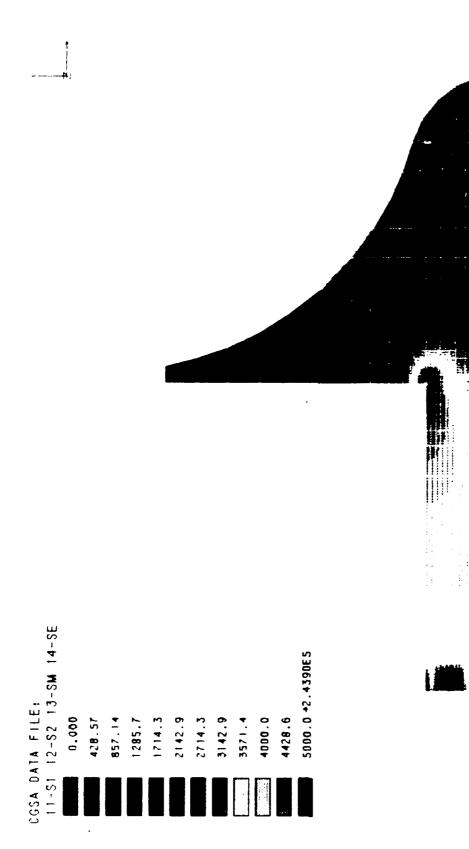


Figure 4-56. (b) Max Shear Stress - Probe w/Chip FEA

4-109

LOADCASE .

The deflected shape of the Probe FEM the chip carrier is shown in Figure 4-54b. Included is a graphical representation of the boundary conditions and an enlarged plot of the solder joint. The deformation of the chip carrier is clearly shown. This deformation increased the compressive loading on the left edge of the solder joint. The compression is shown in the stress contour plots of Figure 4-56.

# 4.8.2.3 Leadless Solder Joint Probe FEA with Chip carrier and Thermal Loads

The leadless solder joint and chip carrier geometry is shown in Figure 4–53b. The material properties are shown in Table 4–3 and the geometry was generated using information from Reference 4–6. The 2–D Probe FEM contains 97 solder elements and 64 chip carrier elements. Symmetric boundary conditions were used at the center of the chip carrier. Motion in the X direction is fixed and motion in the Y direction is free. The applied loading includes imposed displacements which represent the thermal expansion of the PCB in the plus X direction for a temperature differential ( $\Delta T = T_{max} - T_{min}$ ) of 50 degrees C and an applied temperature differential of 50 degrees C. The imposed displacements load is called PXTHERM and the thermal load is called PDTEMP.

The resultant stresses and strains for the 2-D Probe FEA with thermal loads are presented in Table 4-6. When the temperature loads are applied, radically different results are obtained because of the thermal expansion coefficient at the chip carrier/solder interface. This difference is shown in the stress contour plots presented in Figure 4-57.

The deflected shape of this FEM is shown in Figure 4-54c. A graphical representation of the boundary conditions and an enlarged plot of the solder joint is included. The deformation of the chip carrier is clearly shown. The increased bending of the chip carrier was the result of using an average temperature differential of 50 degrees C. The imposed displacements used in the previous leadless solder joint FEA assumed a 53 degree C temperature differential within the chip carrier and a 46 degree temperature differential within the PCB.



LOADCASE - 1 FUNCTION =S1

Figure 4-57. (a) Max Principal Stress - Probe w/Thermal Loads

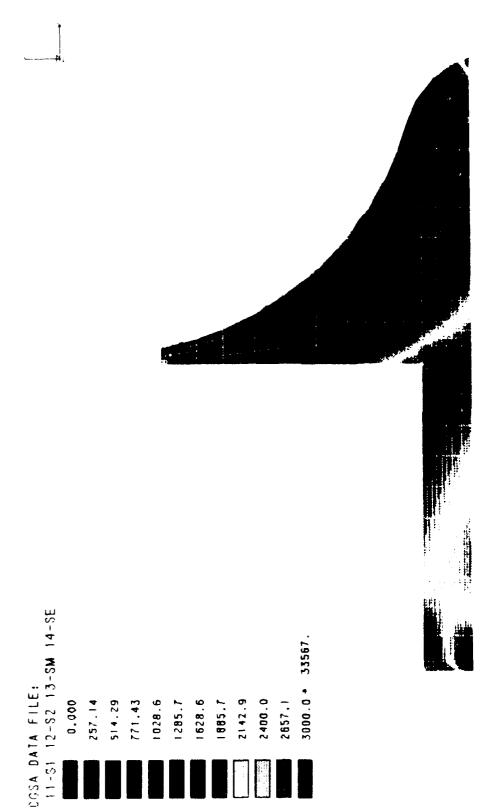


Figure 4-57. (b) Max Shear Stress - Probe w/Thermal Loads

LOADCASE - 1 FUNCTION =SM

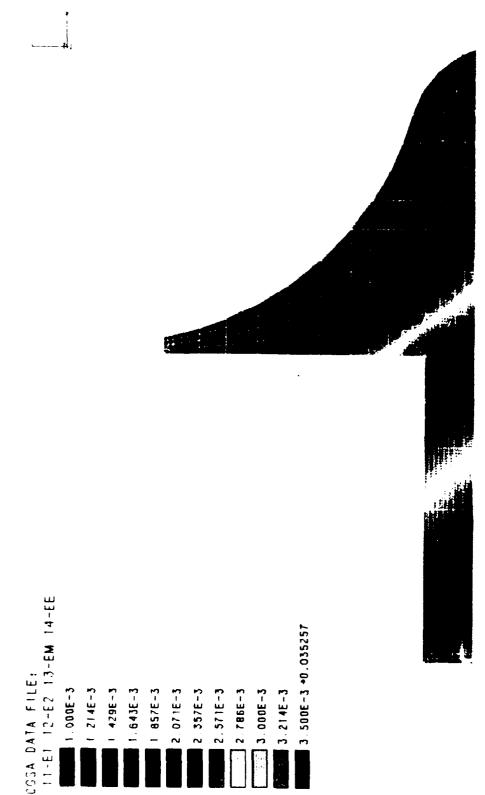


Figure 4-57. (c) Max Principal Strain - Probe w/Thermal Loads

LOADCASE - 1 FUNCTION =S1



Figure 4-57. (d) Max Shear Strain - Probe w/Thermal Loads

LOADCASE - 1 FUNCTION = SM

# 4.8.3 Correlation of FEA Results and Known Failure Locations

Solder joint cracks in the J-lead/solder joint originate either near the outside J-lead/solder intersection within the solder material or from voids within the solder material near the J-lead interface. The cracks propagate around and near the J-lead interface within the solder material. In the models discussed above, the peak stresses do not occur near the outer surface of the solder at the J-lead/solder intersection (See Figures 4-49 through Figure 4-52). This indicates that either voids in the solder material near the J-lead interface or surface flaws near the J-lead/solder interface play a part in the crack initiation process. A circular shaped void will magnify the through stress by a factor of 2 to 4, depending upon the stress distribution around the void. For examples of J-lead/solder joint cracking, see References 4-8 and 4-9. In the 2-D Probe J-lead/solder FEM that allowed thermal expansion in both X and Y directions (Figure 4-52), the maximum total principal strains and maximum shear strains were located in areas where cracking occurs. However, as previously shown, the strains at the outside intersection of the J-lead/solder materials were lower than the maximum principal strains. None of the FEMs included flaws on the solder surface or interior to the solder material.

Solder joint cracks in leadless joints have been shown to originate either near the inside solder/chip carrier interface within the solder material or from voids within the solder material (see References 4–7 and 4–12 for examples of leadless soider joint cracking). These reports show the crack propagating from the inside solder/chip carrier interface, along the interface until reaching the corner and then proceeds normal to the outside solder surface until fracture occurs. This process is fully described in Reference 4–7. The peak stresses/strains will occur at the corner notch as shown in Figure 4–55 through Figure 4–57 and there is the possibility that when subjected to thermal loads, cracking may originate near this corner notch.

#### REFERENCES

- [4-1] Reddy, J.N., "An Introduction to the Finite Element Method"; McGraw-Hill, 1984.
- [4-2] Bathe, K.J., "Finite Element Procedures in Engineering Analysis", Prentice-Hall Inc., Englewood Cliffs, New Jersey, 1982.
- [4-3] Peterson, Rudolph E.; "Stress Concentration Factors"; Wiley, New York, 1974.
- [4-4] Steinberg D.S., "Vibration Analysis For Electronic Equipment", 2nd Edition, Wiley-Interscience, New York, NY, 1988.
- [4-5] Soovere J., Steinberg D.S., and Danduwante B.V., "Vibration Reliability Life Mode! For Avionics," AFWAL-TR-87-3048, September 1987.
- [4-6] Bivens G., "Reliability Assessment Using Finite Element Techniques," RADC-TR-89-281, Nov 1989.
- [4-7] Solomon, H.D.; Brzozowski, V.; Thompson, D.G.; "Prediction of Solder Joint Fatigue Life"; AFWAL-TR-89-4002
- [4-8] Lau, John H.; Harkins, Girvin; Rice, Donald; Kral, Joseph; Wells, Betty; "Experimental & Statistical Analysis of Surface-Mount Technology PLCC Solder Joint Reliability"; IEEE Transactions On Reliability, Vol 37, No. 5, December 1988.
- [4-9] Lau, John H.; Harkins, Girvin; Rice, J. and K. al, Joseph; Wells, Betty; "Experimental Analysis of SMT Solder Joint Control Schanical Fatigue"; IEEE Transactions On Reliability, 1987.
- [4-10] Danduwante B.V., Soovere J., and et al., "Vibration Stress Analysis of Avionics", A. il 1987, AFWAL-TR-87-3023.
- [4–11] Lau J.H. and Harkins C.G., "Thermal–Stress Analysis of SOIC Packages and Interconnections", IEEE Transactions on Components, Hybrids, and Manufacturing Technology, Vol. 11, No 1., December 1988.
- [4-12] Solomon, H.D.; "Low Cycle Fatigue of Surface Mounted Chip Carrier/Printed Wiring Board Joints"; AFWAL-TR-89-4004

- [4–13] Bivens G. and Bocchi W.J., "Reliability Analysis of a Surface Mounted Package using Finite Element Simulation", RADC-TR-87-177, October 1987.
- [4-14] Hall, P.M.; "Creep and Stress Relaxation in Solder Joints in Surface Mounted Chip Carriers"; Proc. IEEE 37th Electronic Components Conference, May 1987, pp. 579-588.
- [4-15] Duncan L.B. et al., "Reliability Assessment of Wafer Scale Integration Using Finite Element Analysis", Hughes Report EDSG Report R972-224, July 1989.
- [4–16] Becker, G.; "Testing and Results to the Mechanical Strength of Solder Joints"; PIC Fall Meeting, November 1979.
- [4-17] Engelmaier, W.; "Fatigue Life of Leadless Chip Carrier Solder Joints During Power Cycling"; Proceeding of the Technical Program of the 2nd Annual International Electronics Packaging Society Conference, November, 1982.
- [4-18] Engelmaier, W.; "Reliability in Surface Mounted Assemblies: Controlling the Thermal Expansion Mismatch Problem"; SMART IV Conference, January, 1988.
- [4-19] Southland J.R., Beatty V.R., and Vitaliano W.J., "Finite Element Analysis of Microelectronic Packages", RADC-TR-82-132, May 1982.

# Chapter 5 RELIABILITY PREDICTIONS

## 5.0 Introduction

The reliability of a comporent is described as its ability to function without failure. This chapter addresses the theories and procedures needed to analyze the failure mechanisms covered in Chapter 3. These failure theories can be used to determine if fracture of the material will occur under operational conditions. This chapter also covers procedures for predicting fatigue life and creep rupture time to failure.

#### 5.1 Deformation

Finite element methods for computing deformation of electronics during vibration and temperature changes were covered in Chapter 4. Deformation results in stresses which can exceed the strength of the material and cause short fatigue lives. This chapter focuses on using these calculated stresses to predict the reliability of electronics.

# 5.2 Fatigue

# 5.2.1 Finite Element Stresses for Fatigue Analysis

The fatigue life of components subjected to bending or axial loads is dictated by the principal stress,  $\sigma_1$ , obtained from FEA. This principal stress represents the maximum normal stress acting on an element. In general, cracks propagate in a direction perpendicular to the direction of the principal stress (Figure 5-1). The principal stresses should be used in predicting the fatigue life of leads connecting the components to the circuit board. Once vibration and thermal stresses are determined from the finite element analysis, a curve of axial stress amplitude ( $\Delta\sigma/2$ ) vs. cycles to failure (N) for the appropriate material should be used to predict fatigue life. Stress vs. life curves for various materials are included in Chapter 2. A different characteristic stress is needed for conditions in which the cracks are forced to propagate under shear deformation. This type of crack is found, for example, along the boundary between a solder joint and a leadless chip carrier (LCC). As the board expands during an increase in temperature, the joint is subjected to

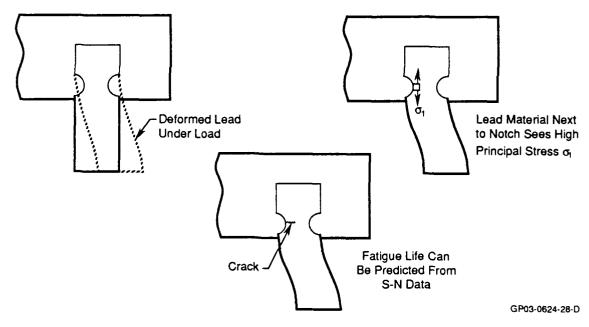


Figure 5-1. Crack Propagation Controlled by Principal Stress

a shear deformation as illustrated in Figure 5–2. The maximum shear stress,  $\tau_{max}$ , should be used in this case for the prediction of fatigue life. If the component analyzed is sheared primarily in one direction, the maximum shear stress is one of the FEA output shear stresses:  $\tau_{xy}$ ,  $\tau_{xz}$ , or  $\tau_{yz}$ . This occurs in the case of the LCC solder joint under temperature changes. If a more complex load condition occurs, the maximum shear stress can be computed from the principal stresses  $\sigma_1$ ,  $\sigma_2$ , and  $\sigma_3$ . The maximum shear stress,  $\tau_{max}$ , is the greater of:

$$\frac{|\sigma_1 - \sigma_2|}{2} \quad \frac{|\sigma_1 - \sigma_3|}{2} \quad \frac{|\sigma_2 - \sigma_3|}{2}$$
 Eq. 1

The fatigue life is then obtained from a plot of shear stress amplitude ( $\Delta\tau/2$ ) versus cycles to failure (N). Under multiaxial load conditions, the use of  $\sigma_i$  or  $\tau_{max}$  to predict fatigue life may be invalid. In these cases, the use of the Von Mises stress is recommended because it contains the three principal stresses. The Von Mises stress computed by FEA can then be used to predict life with material data in terms of Von Mises stress vs. N.

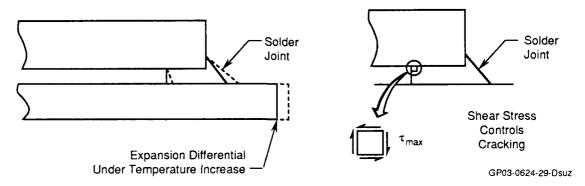


Figure 5-2. Shear Deformation

Fatigue data can also be presented in terms of strain amplitude ( $\Delta \epsilon/2$ ) vs. cycles (N) to failure. This format is typically used when cyclic stresses are high enough to cause yielding and plastic deformation in the critical area. The resulting condition is known as "low cycle fatigue" because failure under high stress occurs in relatively few cycles (less than  $10^5$  cycles). Strain-life data is obtained by controlling the strain as the load is applied. The applied strain is repeated in each cycle until failure of the test specimen occurs. In low cycle fatigue, strain is the controlling parameter because the material is in the plastic region of the stress-strain curve. In this region, small deviations in stress can result in large changes in strain. Therefore, it is difficult to reach a desired point in the plastic region of the stress-strain curve without monitoring strain.

The cycles to failure can be predicted from strain-life data and the strains computed in the finite element analysis. Life predictions for parts under axial or bending loads should be based on the principal strain,  $\epsilon_1$ . The life of materials undergoing shear deformation should be predicted by using the maximum shear strain,  $\gamma_{max}$ . In a two dimensional analysis, the maximum shear strain can be determined from the principal strains  $\epsilon_1$  and  $\epsilon_2$ :

$$\gamma_{\text{max}} = \epsilon_1 - \epsilon_2$$
 Eq. 2

When using strains from finite element analyses, the correct strain needs to be used to predict fatigue life. In Chapter 4, stresses and strains in a J-lead exposed to temperature changes were obtained with PROBE finite element analyses. In several of the analyses, deflections were imposed on the J-lead finite element model to simulate thermal

expansion of the circuit board and the chip carrier. The principal strains obtained in these analyses can be used directly with strain amplitude vs. life data to predict the fatigue life of the material.

In another analysis of the J-lead, the temperature change was imposed on the chip carrier-lead-circuit board model. This allowed the FEA to determine the thermal expansion of the materials without externally imposed displacements. The principal strain output from this PROBE example consists of the mechanical strain and the thermal strain:

$$\epsilon_1 = \epsilon_{\text{mech}} + \epsilon_{\text{thermal}}$$
 Eq. 3

The thermal strain is the product of the material's coefficient of thermal expansion (CTE) and the temperature differential:

$$\epsilon_{\text{thermal}} = \text{CTE} \times \Delta T$$
 Eq. 4

The mechanical strain is caused by the interaction of adjacent materials having different thermal expansion coefficients. Materials with lower CTE prevent the expansion of materials with higher CTE. This results in compressive mechanical strains in the high CTE materials and tensile mechanical strains in the low CTE materials. Mechanical strains cause stresses which lead to fatigue damage. Therefore, when predicting fatigue life, only the mechanical component of  $\epsilon_1$  should be used. The mechanical strain can be extracted from  $\epsilon_1$  a follows:

$$\epsilon_{\text{mech}} = \epsilon_1 - (\text{CTE} \times \Delta T)$$
 Eq. 5

This mechanical strain is then used with strain amplitude vs. life curves to predict the number of cycles to failure. Fatigue life can also be determined by using the FEA principal stress,  $\sigma_1$ , and stress vs. life data. Both procedures will result in equivalent fatigue life predictions. Table 5–1 summarizes the application of the various FEA stresses and strains in fatigue analysis.

TABLE 5-1. APPLICATION OF FEA OUTPUT IN FATIGUE LIFE PREDICTION

Parameter	Symbol	Application	Fatigue Data Needed for Life Prediction
Principal Stress	$\sigma_1$	Materials under axial or bending loads	Δσ/2 vs. N
Max. Shear Stress	$ au_{max}$	Materials under constrained shear deformation	$\Delta  au/2$ vs. N
Principal Strain	€₁	Materials under axial or bending loads	$\Delta \epsilon / 2$ vs. N (low cycle fatigue)
Mechanical Principal Strain	€ <sub>mech</sub>	Materials exposed to temperature changes and analyzed with FEA under applied $\Delta T$	$\Delta$ $\epsilon$ /2 vs. N (low cycle fatigue)
Max. Shear Strain	У <sub>тах</sub>	Materials under constrained shear deformation	$\Delta\gamma/2$ vs. N (low cycle fatigue)

Stress or strain output from finite element analyses can be used in fatigue life prediction with equal accuracy. The choice depends on whether stress-life or strain-life curves are available for the material. Even in the case where only stress-life curves are available, these data can be converted to strain vs. life by using the stress-strain curve for the material.

Table 5-1 assumes that the applied stresses ( $\sigma_1$  or  $\tau_{max}$ ) and strains ( $\varepsilon_1$  or  $\gamma_{max}$ ) are fully reversed during the cycle. For a material under axial loads, the stress at a point should vary from  $\sigma_1$  to  $-\sigma_1$  during each cycle. This condition occurs when the temperature increase above a baseline condition is balanced by a temperature drop of the same magnitude below the baseline. As an example, consider a temperature cycle defined by:

Maximum temperature = 100°C

Minimum temperature = -50°C

Baseline temperature = 25°C (Room temperature)

This temperature cycle will result in fully reversed stresses because the 75°C increase above the baseline equals the 75°C drop below the room temperature condition.

In the case of cycles where the stresses are not fully reversed, the above procedures need to be modified. Methods for analyzing mean stress effects and combinations of vibration and thermal stresses are covered later in this chapter. Load cycles where stresses exceed the yield strength of the material and plastic deformation occurs are also discussed.

# 5.2.2 Fatigue Life Prediction

Once the appropriate stress information is obtained from the finite element analysis, the number of stress cycles which can be sustained by a material can be determined with a fatigue analysis. If the same stress level is attained in each cycle, the stress profile is known as a constant amplitude stress history. The number of cycles to failure can then be determined from a material curve of stress versus cycles as described in Section 3.3. If the stress levels vary from cycle to cycle, the stress profile is a variable amplitude stress history. Variations in stress levels can be caused by variations in maximum temperature, and random vibration, for example. The fatigue damage from the various stress cycles must be accounted for when predicting the fatigue life of the material.

The first step in the analysis requires grouping stress cycles with similar amplitudes together. This results in a series of constant amplitude blocks which represent the stress history. The damage caused by each block of cycles is defined by:

$$\frac{n_i}{N_i}$$
 Eq. 6

where:  $n_i$  = number of cycles at  $\sigma_i$ 

 $N_i$  = number of cycles to failure at  $\sigma_i$ 

This is illustrated in Figure 5-3. Once the damage from each block is determined, Miner's cumulative damage formulation (Reference 5-1) can be used to sum the damage and determine if failure will occur. According to Miner, failure occurs if:

$$\Sigma \frac{n_i}{N_i} \ge 1.0$$
 Eq. 7

Reference 5-2 recommends that 0.7 should be used for electronics instead of 1.0 in Equation 7. This results in more conservative life predictions.

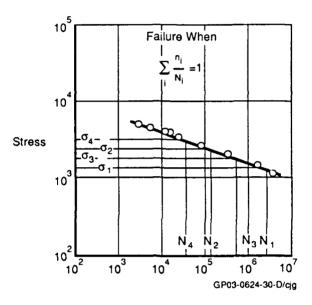


Figure 5-3. Miner's Rule Applied to Counted Effective Strain Ranges

#### 5.2.3 Fatigue Life Predictions Under Combined Stresses

High frequency vibration stresses can occur in combination with slower stress cycles caused by temperature changes or high G aircraft maneuver loads (Figure 5-4). The first step in a fatigue life analysis is to determine the stresses caused by these conditions. A particular temperature, or an RMS vibration level, is selected as the reference condition. The stresses in the electronic material are obtained with a finite element analysis for the reference condition. Each time the component is exposed to this reference condition represents a "load cycle". The magnitude of the load cycles can vary depending on the maximum temperature of each cycle or the level of vibration. Higher temperatures cause

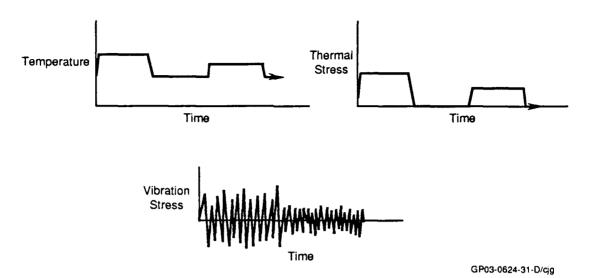


Figure 5-4. Slow Thermal Stresses and High Frequency Vibration Stresses

higher thermal stresses, and higher vibration accelerations lead to greater dynamic stresses. In general, stress is proportional to temperature and vibration level as long as the stresses are elastic (below the yield strength of the material). If stresses exceed the yield strength, then the plastic behavior of the material needs to be considered. The plastic stress analysis was described in Section 4.3.4, and models for analyzing cyclic stresses in the plastic range are covered in Section 5.2.4. Once the stresses are determined for the different conditions, they need to be combined into a load spectrum representing the load history of the component. The fatigue damage caused by each load cycle can then be summed to predict how many cycles can be experienced by the material until failure occurs.

# 5.2.3.1 Independent Vibration and Thermal Stresses

Steinberg (Reference 5–2) has proposed one of the simplest models for combining vibration and thermal stresses. In this model, vibration is assumed to be independent from thermal stresses. The fatigue damage due to vibration and thermal stress cycles are defined as follows:

Vibration Fatigue Damage = 
$$\frac{n_v}{N_v}$$
 Eq. 8

and

Thermal Fatique Damage = 
$$\frac{n_t}{N_t}$$
 Eq. 9

where:  $n_v = number of vibration cycles in a year$ 

 $N_v$  = number of vibration cycles which will cause failure (obtained from stress vs. life S-N data for the material)

 $n_t = number of thermal cycles in a year$ 

 $N_t$  = number of thermal cycles which will cause failure (obtained from S-N curve for the material)

The values of  $N_v$  and  $N_t$  are obtained from material S-N curves similar to Figure 5-5. Constant amplitude stresses on these curves are typically "fully reversed stresses" in which the "R" ratio of minimum/maximum stress equals -1. Random vibration stresses do not contain mean stress or preload. To predict the number of years of operation  $(N_y)$ , the vibration and thermal fatigue damage are then combined as follows:

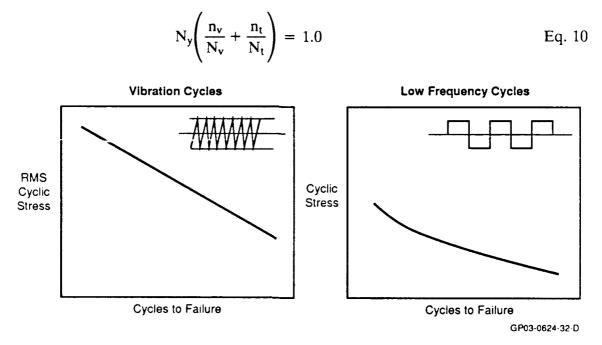


Figure 5-5. Fatigue Data Obtained Under Fully Reversed Stresses

Solving for N<sub>y</sub> gives the fatigue life. Although this model will give an approximate fatigue life for the material, it does not account for simultaneous action of the vibration and thermal cycles illustrated in Figure 5-6.

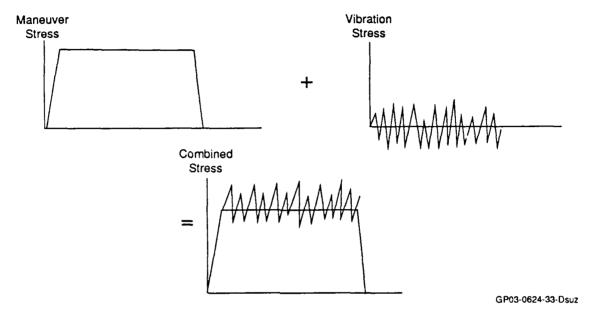


Figure 5-6. Combined Manuever and Vibration Stresses
Without Relaxation or Creep

#### 5.2.3.2 Generating Effective Strain vs. Life Curves

When vibration and temperature cycling occur simultaneously, the thermal stress acts as a static mean stress with vibration stresses superimposed (Figure 5-6). The determination of vibration fatigue damage under this condition is complicated by the limitations of the available S-N data. Most S-N curves for electronic materials have been generated for tests without mean stress. These data need to be modified for use with actual load histories which contain thermal preloads. This data modification is accomplished by first selecting data points from a stress vs. life curve for the particular material (Figure 5-7). The stress values  $(\sigma_{max})$  read from the curve are used to estimate the corresponding values of strain amplitude  $(\Delta \epsilon/2)$ :

$$\frac{\Delta\epsilon}{2} = \frac{\sigma_{\text{max}}}{F}$$
 Eq. 11

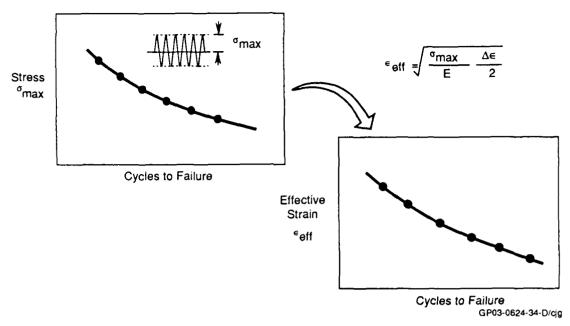


Figure 5-7. Assembly of Effective Strain vs Life Curve

where E is the material modulus of elasticity. Equation 11 is not valid if the maximum stress exceeds the yield strength of the material. If yielding occurs, the strains ( $\Delta \epsilon/2$ ) need to be estimated from the cyclic stress vs. strain curve for the material as illustrated in Figure 5–8. The maximum stress ( $\sigma_{max}$ ), the strain ( $\Delta \epsilon/2$ ), and E are then substituted into the 'following effective strain equation developed by Smith, Watson and Topper (Reference 5–3):

$$\epsilon_{\text{eff}} = \sqrt{\frac{\sigma_{\text{max}}}{E}} \frac{\Delta \epsilon}{2}$$
 Eq.12

An effective strain is computed for each point selected in the original S-N curve to form a new  $\varepsilon_{eff}$  vs. life curve. In the final step in the fatigue life prediction procedure, the stresses listed in the stress history are converted into effective strains. The fatigue damage caused by each stress cycle can then be determined from the  $\varepsilon_{eff}$  vs. life curve.

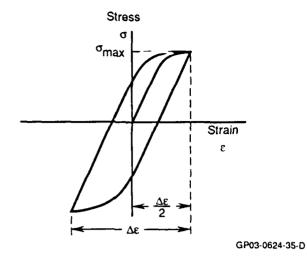


Figure 5-8. The Strain Amplitude  $\Delta\epsilon/2$  Can Be Obtained From the Stress-Strain Curve

# 5.2.3.3 Generating Effective Strain Histories

Vibration load histories are composed of high frequency cycles with random amplitude. Reference 5–2 suggests that random amplitude cycles can be modeled with a Gaussian distribution of maximum and minimum stress levels (Figure 5–9). The amplitudes in a Gaussian distribution are arranged as follows:

68.3% of cycles are between 0 and 1 RMS 27.1% of cycles are between 1 and 2 RMS 4.3% of cycles are between 2 and 3 RMS

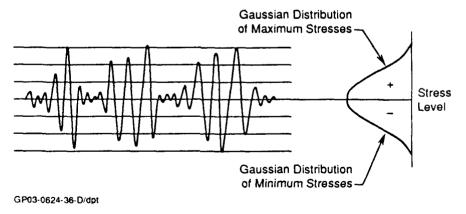


Figure 5-9. Gaussian Distribution of Stress Amplitudes

A Rayleigh distribution an also be used during vibration analysis (Figure 5-10) to determine the peak stress distributions (Reference 5-4). The stress peaks in a Rayleigh distribution are broken down as follows:

39.3% of peaks are between 0 and 1 RMS 47.2% of peaks are between 1 and 2 RMS 12.3% of peaks are between 2 and 3 RMS 1.2% of peaks are between 3 and 4 RMS

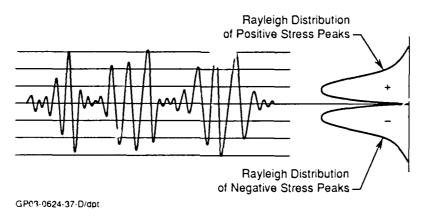


Figure 5-10. Rayleigh Distribution of Stress Peaks

With these assumed distributions, the random vibration cycles can be represented by a much simpler model composed of four blocks of constant amplitude cycles (Figure 5–11). The maximum and minimum stresses are defined for each block as:

$$(\sigma_{\text{max}})_1 = \sigma_{\text{thermal}} + \sigma_{\text{RMS}}$$
  
 $(\sigma_{\text{min}})_1 = \sigma_{\text{thermal}} - \sigma_{\text{RMS}}$  Eq. 13

$$(\sigma_{\text{max}})_2 = \sigma_{\text{thermal}} + 2 * \sigma_{\text{RMS}}$$

$$(\sigma_{\text{min}})_2 = \sigma_{\text{thermal}} - 2 * \sigma_{\text{RMS}}$$
Eq. 14

$$(\sigma_{\text{max}})_3 = \sigma_{\text{thermal}} + 3 * \sigma_{\text{KMS}}$$
  
 $(\sigma_{\text{min}})_3 = \sigma_{\text{thermal}} - 3 * \sigma_{\text{RMS}}$  Eq. 15

$$(\sigma_{\text{max}})_4 = \sigma_{\text{thermal}} + 4 * \sigma_{\text{RMS}}$$
  
 $(\sigma_{\text{min}})_4 = \sigma_{\text{thermal}} - 4 * \sigma_{\text{RMS}}$  Fq. 16

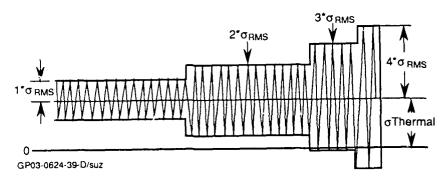


Figure 5-11. Model of Random Vibration With Blocks of Constant Amplitude Cycles

where:  $\sigma_{thermal}$  = thermal mean stress

 $\sigma_{RMS}$  = root-mean-square of the vibration stress

The strain amplitude of each block can be determined with the following procedure:

$$(\epsilon_{\text{max}})_{i} = \frac{(\sigma_{\text{max}})_{i}}{E}$$
 Eq. 17

$$(\epsilon_{\min})_i = \frac{(\sigma_{\min})_i}{E}$$
 Eq. 18

where i = 1, 2, 3, or 4 RMS levels. The strain amplitude is then:

$$(\Delta \epsilon)_i = (\epsilon_{\text{max}})_i - (\epsilon_{\text{min}})_i$$
 Eq. 19

The effective strain characterizing each block of constant amplitude cycles is computed with Equation 12:

$$(\epsilon_{\rm eff})_{\rm i} = \sqrt{\frac{(\sigma_{\rm max})_{\rm i}}{\rm E}} \frac{(\Delta \epsilon)_{\rm i}}{2}$$
 Eq. 20

Finally, the fatigue damage due to each block of cycles is:

Fatigue Damage<sub>1</sub> = 
$$\frac{n_i}{N_1}$$
 Eq. 21

where:  $n_1$  = number of vibration cycles of amplitude i\*RMS which occur in a year  $N_1$  = number of cycles of amplitude i\*RMS which will cause failure (obtained from  $\epsilon_{eff}$  vs. N curve)

As an example, consider a component mounted on a PCB which will vibrate 100 hours in a year. If the first mode natural frequency (of the PCB) is 200 Hz, the number of cycles with  $1*\sigma_{RMS}$  amplitude is defined by the Rayleigh distribution:

$$n_1 = 0.393 * 100 \text{ Hrs } * 3600 \text{ sec/Hr} * 200 \text{ cycles/sec}$$
  
= 2.83 \* 10<sup>7</sup> cycles in a year

The value of  $N_1$  is obtained from the  $\epsilon_{eff}$  vs. life curve at an effective strain  $(\epsilon_{eff})_1$  as illustrated in Figure 5–12. Similar computations can be repeated for the other blocks of amplitude  $2*\sigma_{RMS}$ ,  $3*\sigma_{RMS}$ , and  $4*\sigma_{RMS}$ . To predict the number of years of operation  $(N_v)$ , the damage due to each block is added:

$$N_{v}\left(\sum_{i=1}^{4} \frac{n_{i}}{N_{i}}\right) = 1.0$$
 Eq. 23

Solving for  $N_y$  gives the fatigue life of the material in terms of years of operation.

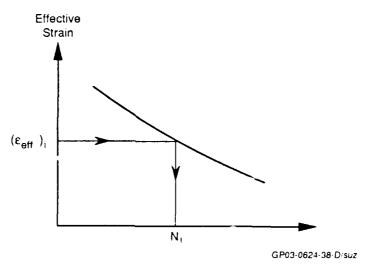


Figure 5-12. Effective Strain Is Used to Predict Fatique Life

The way in which the stresses are combined depends on the material and load condition. When the analysis focuses on materials which do not creep the thermal stresses are sustained during the entire temperature cycle. The procedures described above are then valid.

#### 5.2.4 Cyclic Plastic Stresses

As long as the applied stresses do not exceed the material yield strength, the cyclic stress-strain behavior will remain linear (Figure 5-13). However, if the stress exceeds the yield strength, plastic deformation occurs, and the material will follow its stress-strain curve to the peak of the cycle (Figure 5-14).

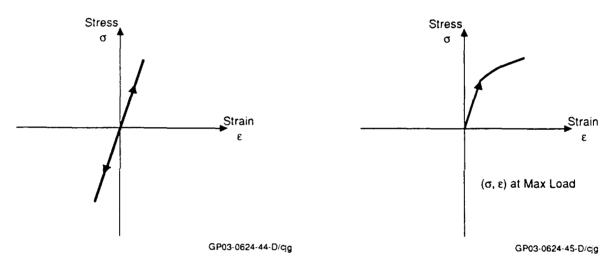


Figure 5-13. Linear Elastic Cyclic Stress-Strain Behavior

Figure 5-14. Plastic Stress-Strain Condition at the Peak of the Cycle

Section 4.3.4 described procedures for estimating plastic stresses from linear elastic finite element analyses. One procedure assumes that the actual plastic strain equals the strain computed with finite element analysis. The plastic stress is read from the stress–strain curve at the given strain. A second more conservative estimate can be obtained by using Neuber's rule which assumes that:

$$(\sigma_{\text{max}}\epsilon_{\text{max}})_{\text{actual}} = (\sigma_{\text{max}}\epsilon_{\text{max}})_{\text{FEA}}$$
 Eq. 24

The actual plastic stress and strain combination must fall on the curve of  $\sigma$  vs.  $\epsilon$ . These procedures are used to find the stress and strain at the peak of the load cycle. A similar procedure can be used to determine the stress and strain state under reversed loads. Just as the material follows its stress-strain curve during loading, the material follows a set path in the unloading part of the cycle (Figure 5-15). This path, known as the hysteresis curve, describes the cyclic stress-strain behavior in the plastic range (Figure 5-16). The hysteresis curve for a material can be determined from cyclic stress-strain characterization tests. If data is not available, the hysteresis curve can be approximated

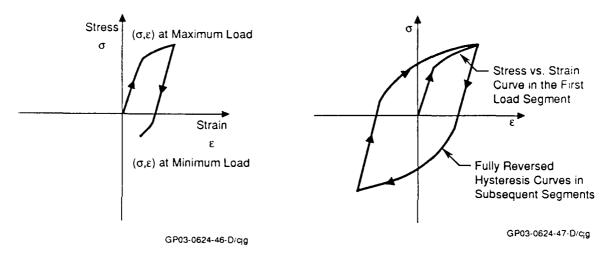


Figure 5–15. Stress-Strain Behavior During a Reversed Load

Figure 5-16. Hysteresis Stress-Strain Curves Under Fully Reversed Cycles

from the stress-strain curve. One approach is to assume that the hysteresis curve is similar to the stress-strain curve, but twice as large (Reference 5-5). To generate the curve,  $\sigma$  and  $\epsilon$  values of selected data points on the stress-strain curve are multiplied by two:

$$\sigma_{\text{hys}} = 2 \times \sigma$$
 $\epsilon_{\text{hys}} = 2 \times \epsilon$ 
Eq. 25

These data points then describe the hysteresis curve as illustrated in Figure 5-17.

Once the hysteresis curve is established, it can be used to determine the change in stress ( $\Delta \sigma$ ) and strain ( $\Delta \epsilon$ ) during the cycle illustrated in Figure 5–18. In this figure, the origin of the "inverted" hysteresis curve is at the point of load reversal. If plasticity oc-

curs during the unloading part of the cycle, Neuber's rule can be used once again to obtain the actual state of stress and strain:

$$(\Delta \sigma \times \Delta \epsilon)_{\text{actual}} = (\Delta \sigma \times \Delta \epsilon)_{\text{FEA}}$$
 Eq. 26

where: 
$$\Delta \sigma_{\text{FEA}} = (\sigma_{\text{max}} - \sigma_{\text{min}})_{\text{FEA}}$$
 Eq. 27

$$\Delta \epsilon_{\text{FEA}} = \Delta \sigma_{\text{FEA}} / E$$
 Eq. 28

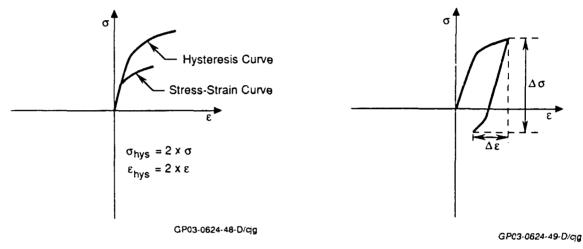


Figure 5-17. Hysteresis Curve Generated From the Material Stress-Strain Curve

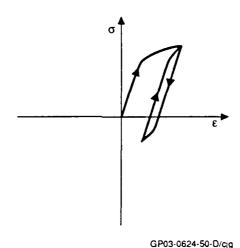
Figure 5-18. Cyclic Stress-Strain Range

The actual change in stress  $\Delta \sigma$  and the change in strain  $\Delta \varepsilon$  are obtained from the hysteresis curve at the point of the curve which satisfies Equation 26:

$$\Delta \sigma_{\rm actual} = \sigma_{\rm hys}$$
 Eq. 29

$$\Delta \epsilon_{\rm actual} = \epsilon_{\rm hys}$$
 Eq. 30

Subsequent constant amplitude load cycles will reach the actual maximum stress and strain and will have the same stress and strain range as illustrated in Figure 5–19.



a. 65 652 v 65 5/6

Figure 5-19. Stress-Strain Loop During Constant Amplitude Cycles

# 5.3 Creep and Stress Relaxation

# 5.3.1 Creep Failure Under Constant Load

Solder is an example of a material which undergoes time dependent deformation, or creep, under sustained stress. This type of material will continue to deform until rupture occurs. In general, the higher the stress the shorter is the time to failure. Figure 5–20 illustrates creep rupture data for 60–40 solder at various temperatures (Reference 5–6). To generate the data in Figure 5–20, the stress in each test was held constant until failure of the specimen occurred.

After completing a finite element analysis, the time to failure can be determined from Figure 5–20 at the calculated stress acting in the material. This type of analysis is applicable to cases where the stress level is maintained continuously. This includes electronics which remain on for significant periods of time.

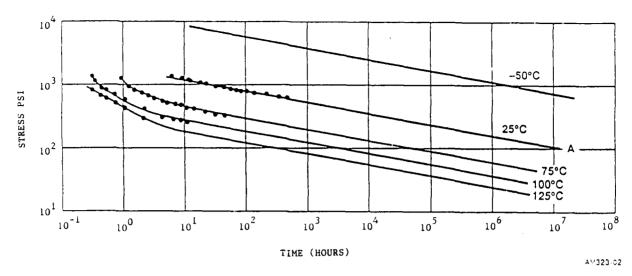


Figure 5-20. Creep Rupture Stress of Solder (60SN - 40 Pb)

# 5.3.2 Combination of Creep/Stress Relaxation and Fatigue

When predicting the fatigue life of solder, the load history model must account for creep and stress relaxation (Figure 5-21). After power-on, the heat generated by the component increases the temperature of the case. As the heat dissipates into the board, board temperatures increase, but at a lower rate than the case temperature increase (Reference 5-7). The chip carrier, therefore, expands first as illustrated by Condition 2 in Figure 5-21. This results in solder thermal stresses. As the maximum temperature of the case is reached, the board catches up in temperature. Because of the higher coefficient of thermal expansion, the board expands more than the chip carrier, which results in the reversed stresses at Condition 3. The board and the component remain expanded as long as the maximum temperatures are maintained. Under this constant solder displacement, the stresses decrease or relax as discussed in Section 3.4. The stresses decrease very rapidly to Condition 4 in Figure 5-21. Upon power-off, the temperature in the case decreases rapidly as the remaining heat dissipates into the board. This causes a contraction of the case before the board begins to contract, and creates stresses in the solder (Condition 5). The components and the board eventually return to their original dimensions as the temperatures decrease to the original levels before power on. This results in reversed solder stresses (Condition 6), which will also relax over time to Condition 7.

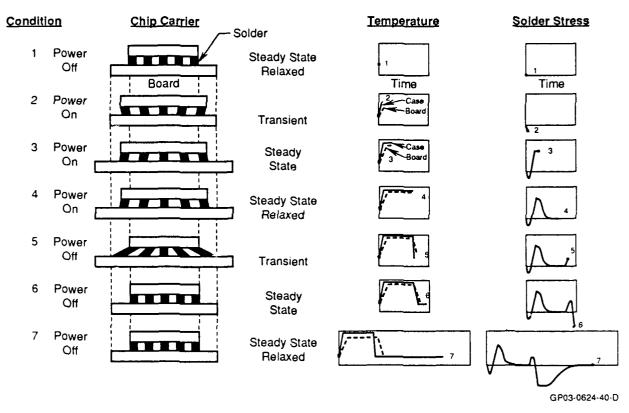


Figure 5-21. Relaxation of Thermal Stress in Solder

Low thermal stress cycles can be ignored to simplify the above thermal stress profile. This truncation procedure is used to filter out cycles which cause negligible fatigue damage. Examples of these type in Figure 5–21 include the stress cycles caused by transient temperature changes during power on and power off. Although the component case heats up first during power on, the difference in temperature between the case and the PCB is generally low. Initial expansion of the case is also small because of its low coefficient of thermal expansion. Deleting the stress cycle between Conditions 1 and 2 and the cycle between Conditions 4 and 5 results in the simpler thermal stress profile in Figure 5–22.

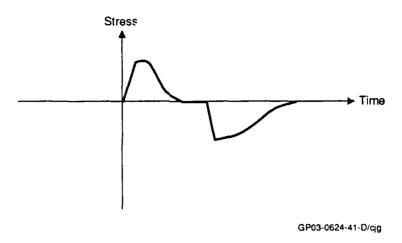


Figure 5-22. Simplified Thermal Stress Model

If vibration occurs while the electronics are on, the majority of vibration will occur with the thermal stresses close to zero (Figure 5-23). Therefore, the vibration and thermal stresses are essentially independent as in Figure 5-24, and their effect on fatigue life can be analyzed with the model discussed in Section 5.2.3.1.

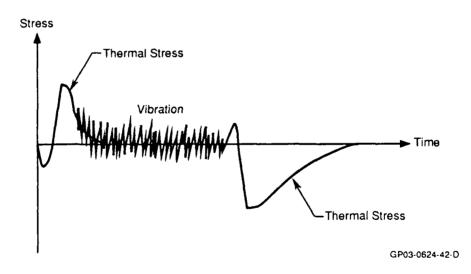


Figure 5-23. Combined Vibration Stresses and Thermal Stresses in Solder

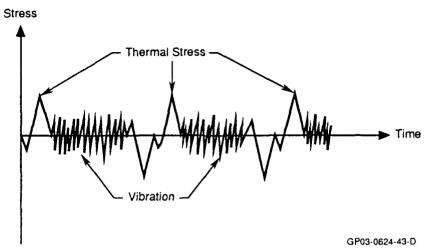


Figure 5-24. Soider Stress History Model

# 5.4 Fracture

#### 5.4.1 Brittle Fracture

Brittle materials, such as ceramics, undergo little or no plastic permanent deformation under large stress (Figure 5-25). Fracture (physical separation of a component into two or more parts) occurs when the stress in the critical area reaches the ultimate strength of the material. To check if failure will occur under the operational conditions, the stress ( $\sigma$ ) computed with the finite element analysis should be compared with the ultimate strength ( $\sigma_{ult}$ ). The material will fail if:

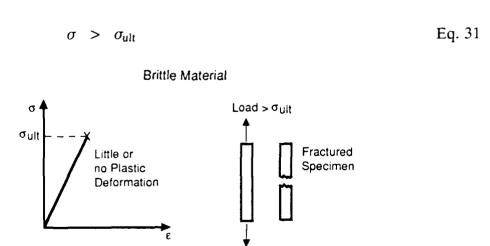


Figure 5-25. Brittle Fracture

#### 5.4.2 Ductile Fracture

As discussed in Chapter 3, ductile materials undergo localized plastic deformation when the stress in the critical area exceeds the yield strength. As the load increases, larger volume of plastic zone increases until the entire cross section has yielded. Failure occurs when the ultimate strength is exceeded across the entire section. These ductile failures are characterized by highly deformed broken parts (Figure 5–26). Equation 31 can be used once again to determine if ductile failure will occur under the operational environment. However, the stresses along the entire cross section must exceed the ultimate strength. If only a localized region experiences large stress, plastic yielding will prevent fracture.

If stresses are lower than the ultimate strength of the material, fracture can still occur under fatigue or creep. Failure from repetitive load cycles occurs when fatigue cracks grow to a critical size which results in sudden fracture of the part. A sustained load acting on a creep sensitive material can eventually result in fracture of the component. Fatigue and creep failure theories and analysis procedures were covered in Sections 5.2 and 5.3, respectively.

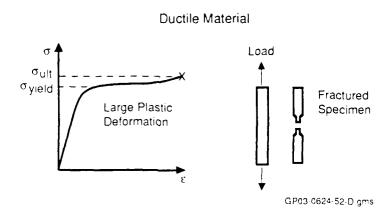


Figure 5-26. Ductile Fracture

Leads and solder joints in which fracture is caused by fatigue show little permanent plastic deformation. None of the large scale deformation, which ductile materials experience during a single large load, occurs in fatigue failures. Because of this, fatigue failures

are sometimes called "brittle failures" although the material may be ductile. The term brittle failure in reference to fatigue is inaccurate, since localized plastic zones do occur around fatigue crack tips (Figure 5–27).

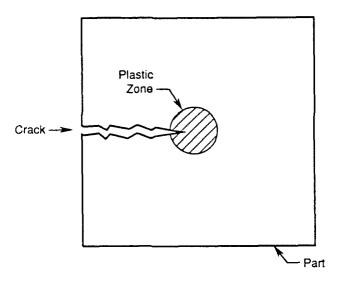


Figure 5-27. Plastic Zone Surrounding a Crack Tip

# 5.5 Buckling

Buckling can occur during out of plane deformation of a printed circuit board. The leads connecting components to the board act as columns which are loaded in tension and compression (Figure 5–28). To determine if buckling will occur, the loads acting on the leads are first obtained with finite element analysis. The critical buckling load can be computed by using the following formula for a fixed-fixed beam (Reference 5–8):

$$F_{cr} = \frac{4\pi^2 E I}{L^2}$$
 Eq. 32

where: E = Young's Modulus

I = Moment of Inertia - Beam Cross Section

L = Length of Beam

of the leads buckle, loads get redistributed to the other leads on the component. This is a very complicated problem which may require a buckling finite element analysis of the multiple lead system to obtain actual deformation. Since the lead can return to its original shape upon unloading, buckling of a lead may not necessarily imply failure of a lead. However, a buckled lead may impose large deformations on the solder joint, and may result in solder fatigue damage. A finite element analysis of the deflected solder joint can then be used to determine stresses in the solder.

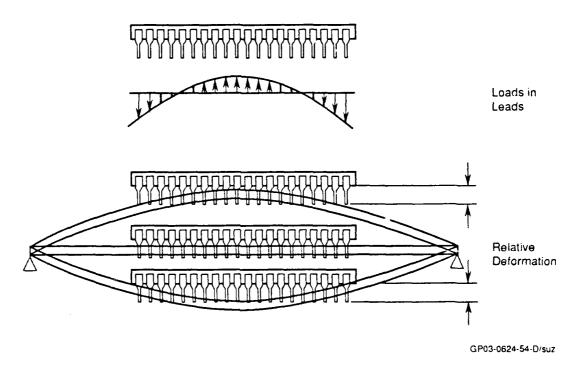


Figure 5-28. Out of Plane Board Deflections Can Cause Buckling of Leads

#### References

- [5–1] Miner, M.A., "Cumulative Damage in Fatigue," Tran. ASME, J. Appl. Mech., Vol. 67, Sept. 1945.
- [5-2] Steinberg, D.S., "Tools Available for Implementing AVIP," Presented at the 9th Annual IEEE/AESS Symposium, Dayton, OH, 30 Nov 1988.
- [5–3] Smith, K.N., Waison, P., and Topper, T.H., "A Stress-Strain Function for the Fatigue of Metals," J.Mater., Vol. 5, No. 4, Dec. 1970, p.767.
- [5-4] Harbison, S.T., Perez, R., Smith, H.G., Saff, C.R., "Development of Techniques for Incorporating Buffet Loads in Fatigue Design Spectra," NADC Report, 1991.
- [5-5] Fuchs, H.O., Stephens, R.I., "Metal Fatigue in Engineering," John Wiley and Sons, 1980, p.137.
- [5-6] Data collected by B. Steffens and R. Lee, Martin Marietta Electronic Systems.
- [5-7] Engelmaier, W., "Fatigue Life of Leadless Chip Carrier Solder Joints During Power Cycling," Proc. of the Technical Program of the 2nd Annual International Electronics Packaging Society Conf., San Diego, CA, November 1982.
- [5-8] Stevens, K.K., "Statics and Strength of Materials," Prentice-Hall, Inc., 1979.

# Chapter 6 RELIABILITY APPLICATIONS

## 6.0 Introduction

This chapter describes how the results of finite element analyses are used to predict fatigue life and reliability using the procedures from Chapter 5. Several examples are included to illustrate the procedures. The first two examples, J-lead/solder joint and the leadless chip carrier solder joint, include the finite element results documented in Chapter 4. The third example describes a life prediction of a dual-in-line package lead/solder connection. The stresses used in this example were obtained using non-finite element methods to illustrate alternate analysis procedures. The fourth example covers a driver amplifier using MMIC technology (gallium arsenide chip and gold metallization with monolithic circuitry containing six transistor cells). This component is part of a Transmit/Receive Radar Module. The life of the gold material exposed to thermal stresses is predicted in this example. The fifth example covers procedures for checking the likelihood of buckling in leads subjected to compression loads during vibration.

# 6.1 J-Lead Fatigue Analysis

The following is a list of the basic parameters used in this J-lead analysis:

Failure Mechanism - Fatigue, Creep and Stress Relaxation

Failure Theory – Miner's Rule on Cumulative Faiigue Damage

Device - Flight Control Computer Printed Circuit Board

Component - 68 J-Lead Surface Mounted Chip Carrier

Material - Kovar and Solder

Environment - On-Off Temperature Cycles and Aircraft Vibration

### 6.1.1 Thermal Fatigue Analysis

A J-lead/solder joint finite element analysis was completed to determine the stress in critical locations. Different finite element codes and boundary conditions were used to compare various ways of analyzing the same problem. These finite element analyses,

described in Chapter 4, simulated a temperature increase of approximately 50 degrees C. From the various J-lead finite element analyses, one was chosen to illustrate the fatigue life prediction procedures. This analysis consisted of a PROBE model of the chip carrier. J-lead, solder joint, and circuit board under an imposed temperature change (Figure 6-1). The upper lead elbow and the solder/lead interface were selected as critical locations where fatigue failure could occur (Figure 6-2), since the lead elbow has the highest thermal stress in the lead material and the solder experiences large thermal stress in the solder/lead interface, a known failure location.

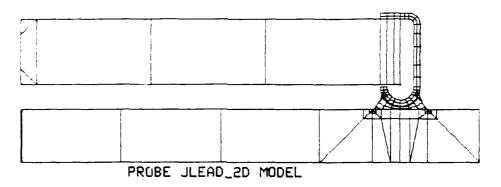


Figure 6-1. J-Lead/Solder Joint Geometry

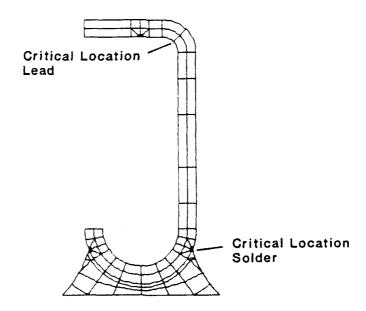


Figure 6-2. Critical Areas Analyzed in the Thermal Cycle Reliability Assessment

## 6.1.1.1 Lead Material Fatigue

The upper lead bend experiences a principal stress,  $\sigma_1$ , of 1400 psi because of the 50°C temperature increase. The maximum temperature is maintained long enough for complete stress relaxation and creep in the solder, allowing the lead to return to its original shape. As a result, the stress in the lead material decreases to zero.

As the temperature decreases to its initial level, the lead is deformed in the opposite direction and reversed stresses equal to -1400 psi occur. The original temperature is maintained long enough for complete stress relaxation and creep in the solder, once again resulting in zero stress in the lead after a period of time has elapsed.

This stress cycle consists of fully reversed stress (1400 to -1400 psi) and a stress ratio of -1. Figure 6-3 (Reference 6-1) illustrates the lead material fatigue data used to predict the life. According to this figure, the lead material can sustain more than 10<sup>9</sup> cycles without failure.

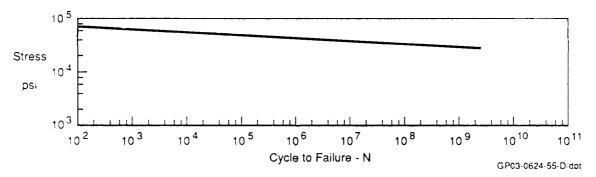


Figure 6-3. Constant Amplitude S-N Fatigue Curve for Electrical Lead Wire, Type D, Type K, Reversed Bending

#### 6.1.1.2 Solder Fatigue

The solder experiences a maximum shear stress of 1240 psi near the solder/lead interface. The maximum temperature is maintained long enough for complete stress relaxation and creep in the solder (Figure 6-4). As the temperature decreases to its initial level, a reversed stress equal to -1240 psi occurs in the solder. Stress relaxation and creep causes a return to the original zero stress and strain state. The stress-strain behavior illustrated in Figure 6-4 was described by Engelmaier (Reference 6-2).

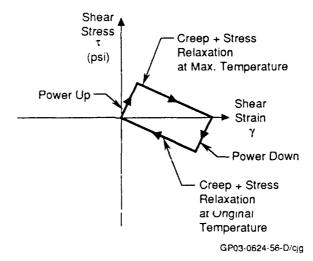


Figure 6-4. Solder Stress-Strain Cycle in a J-Lead Connection

The fully reversed stress cycles with amplitude of 1240 psi will result in a fatigue life of 700,000 cycles, as read from the S-N curve in Figure 6-5. The stress vs. life curve in Figure 6-5 was generated from strain vs. life data in References 6-3 and 6-4.

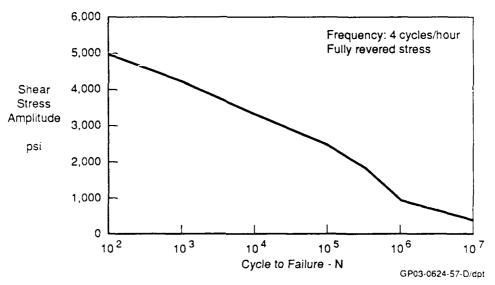


Figure 6-5. S-N Curve for 63-37 Solder at Room Temperature

## 6.1.2 Vibration Fatigue Analysis

A J-lead/solder joint finite element analysis was completed to determine the stress in critical locations. The ABAQUS finite element code was used to determine deformations and stresses in the lead and solder joint material. These 3-dimensional finite element analyses, described in Chapter 4, simulated a vibration environment.

Based on the finite element results, two critical locations were selected for fatigue life assessment. Figure 6–6 illustrates a side view of the 3–D finite element model and the critical locations. The first critical area is located in the Kovar material where the lead first meets the chip carrier. Large vibration stresses in the Kovar lead material occur in this region. The second possible failure area occurs in the solder near the solder/lead interface.

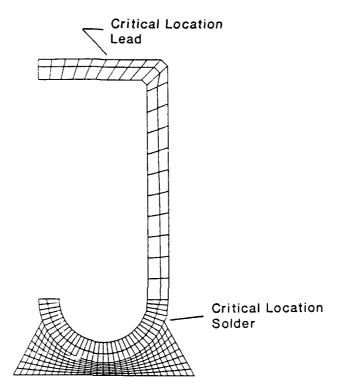


Figure 6-6. Critical Areas Analyzed in the Vibration Reliability Assessment

## 6.1.2.1 Lead Material Fatigue

The principal stress,  $\sigma_1$ , in the lead critical region was computed with ABAQUS FEA to be 14,390 psi RMS. Because of stress relaxation, thermal stresses are approximately zero by the time vibration starts. As a result, the vibration stresses are fully reversed. Figure 6–7 (from Reference 6.1) presents random vibration RMS stress vs. cycles to failure data for lead material. The fatigue life corresponding to a 14,390 psi RMS stress is:

 $N = 4 \times 10^8$  cycles

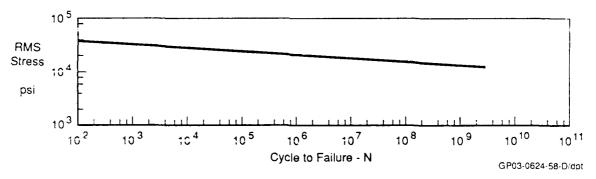


Figure 6-7. Random Amplitude S-N Fatigue Curve for Electrical Lead Wire, Type D, Type K, Reversed Bending

If no random vibration fatigue data is available for the material, a life prediction based on constant amplitude fatigue data can still be performed. This procedure, described in Section 5.3.2, consists of assuming a Gaussian distribution of random vibration stresses and modeling this distribution with the following constant amplitude blocks of stress:

68.3% of cycles with amplitude = 
$$\sigma_{RMS}$$
  
27.1% of cycles with amplitude =  $2 \times \sigma_{RMS}$   
4.3% of cycles with amplitude =  $3 \times \sigma_{RMS}$ 

This results in the following peak stresses for this example:

$$(\sigma_{\text{max}})_1 = \sigma_{\text{RMS}} = 14,390 \text{ psi}$$
  
 $(\sigma_{\text{max}})_2 = 2 \text{ x } \sigma_{\text{RMS}} = 28,780 \text{ psi}$   
 $(\sigma_{\text{max}})_3 = 3 \text{ x } \sigma_{\text{RMS}} = 43,170 \text{ psi}$ 

The number of cycles to failure at each stress level can be read from Figure 6-3 (Reference 6-1):

At 
$$(\sigma_{max})_1$$
,  $N_1 = 1.2 \times 10^{13}$  cycles  
At  $(\sigma_{max})_2$ ,  $N_2 = 6.0 \times 10^8$  cycles  
At  $(\sigma_{max})_3$ ,  $N_3 = 1.8 \times 10^6$  cycles

Failure is defined to occur when:

$$\frac{n_1}{N_1} + \frac{n_2}{N_2} + \frac{n_3}{N_3} \ge 1.0$$
 Eq. 2

where  $n_i$  (i = 1, 2, 3) is the number of cycles at each  $(\sigma_{max})_i$ . The total number of cycles to failure is:

$$N = n_1 + n_2 + n_3$$
 Eq. 3

From the assumed Gaussian distribution:

$$n_1 = 0.683 \text{ x N}$$
 Eq. 4

$$n_2 = 0.271 \text{ x N}$$
 Eq. 5

$$n_3 = 0.043 \text{ x N}$$
 Eq. 5

Substituting into Equation (2):

$$N\left(\frac{0.683}{N_1} + \frac{0.271}{N_2} + \frac{0.043}{N_3}\right) = 1.0$$
 Eq. 7

and solving for N gives the number of cycles to failure:

$$N = \left(\frac{0.683}{N_1} + \frac{0.271}{N_2} + \frac{0.043}{N_3}\right)^{-1}$$
 Eq. 8

Substituting the values of Ni from Equation 1 into Equation 8 results in the following life prediction for this example:

$$N = \left(\frac{0.683}{1.2 \times 10^{13}} + \frac{0.271}{6.0 \times 10^8} + \frac{0.043}{1.8 \times 10^6}\right)^{-1}$$
 Eq. 9

This life prediction using constant amplitude fatigue data was shorter than the prediction of  $4.0 \times 10^8$  cycles based on random vibration data. The constant amplitude model was designed to be conservative to cover inaccuracies inherent with the assumed Gaussian distribution. This was achieved by assuming that any cycle with amplitude between 0 and  $\sigma_{RMS}$ , has an amplitude of  $\sigma_{RMS}$ . Any between  $\sigma_{RMS}$  and  $2 \times \sigma_{RMS}$ , has an amplitude of  $2 \times \sigma_{RMS}$ . Similar assumptions apply to  $3 \times \sigma_{RMS}$ , resulting in a conservative model.

#### 6.1.2.2 Solder Fatigue

From the same FEA analysis, the maximum shear stress,  $\tau_{\text{max}}$ , in the solder critical region was computed to be 600 psi RMS. Once again, thermal stress relaxation results in fully reversed vibration stresses. Figure 6-8 (from Reference 6-1) presents random vibration RMS stress vs. cycles to failure data for solder material. The fatigue life corresponding to a 600 psi RMS stress is:

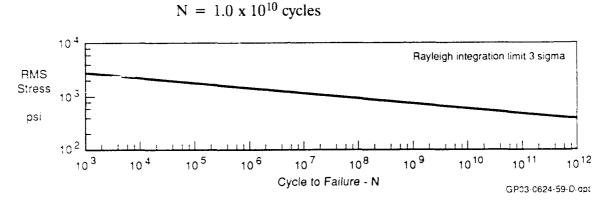


Figure 6-8. Random Amplitude S-N Fatigue Curve for Soft Solder (37% Lead - 63% Tin), Reversed Shear

The constant amplitude procedure is also used in this example to compare with results using the random stress fatigue data. The maximum shear stresses for the Gaussian in this example are:

$$(\tau_{\text{max}})_1 = \tau_{\text{RMS}} = 600 \text{ psi}$$
  
 $(\tau_{\text{max}})_2 = 2 \text{ x } \tau_{\text{RMS}} = 1200 \text{ psi}$   
 $(\tau_{\text{max}})_3 = 3 \text{ x } \tau_{\text{RMS}} = 1800 \text{ psi}$ 

The number of cycles to failure at each stress level can be read from Figure 6-9 (Reference 6-1):

At 
$$(\tau_{\text{max}})_1$$
,  $N_1 = 6.0 \times 10^{13}$  cycles  
At  $(\tau_{\text{max}})_2$ ,  $N_2 = 3.5 \times 10^{10}$  cycles  
Eq. 10  
At  $(\tau_{\text{max}})_3$ ,  $N_3 = 4.4 \times 10^8$ 

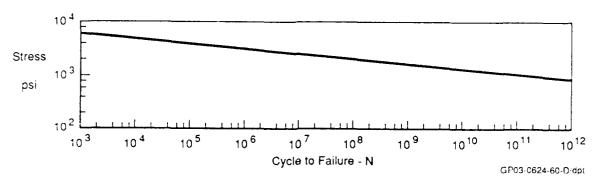


Figure 6- 9. Constant Amplitude S-N Fatigue Curve for Soft Solder (37% Lead - 63% Tin), Reversed Shear

Substituting into Equation 8:

$$N = \left(\frac{0.683}{6.0 \times 10^{13}} + \frac{0.271}{3.5 \times 10^{10}} + \frac{0.043}{4.4 \times 10^8}\right)^{-1}$$
 Eq. 11  
= 9.5 x 10<sup>9</sup> cycles

Once again, the life prediction using the constant amplitude method is shorter than the prediction based on random stress fatigue data.

# 6.2 LCC Solder Joint Thermal Fatigue Analysis

The following is a list of the basic parameters used in this leadless chip carrier analysis.

Failure Mechanism - Low Cycle Fatigue Cracking

Failure Theory - Strain vs. Cycles to Failure

Device - Flight Control Computer Printed Circuit Board

Component - Leadless Chip Carrier with 68 Solder Joints

Material – Solder 63–37

Environment – On-Off Temperature Cycles

# 6.2.1 Thermal Stress Analysis

A leadless chip carrier solder joint finite element analysis was completed to determine the stress in critical locations. Different finite element codes and boundary conditions were used to compare various ways of analyzing the same problem. These finite element analyses, described in Chapter 4, simulated a temperature increase of approximately 50 degrees C. From the various solder joint finite element analyses, one was chosen to illustrate the fatigue life prediction procedures. This analysis consisted of a PROBE model of the chip carrier and solder joint under an imposed temperature change (Figure 6–10). The critical location in the solder/chip carrier interface was located near the corner of the chip carrier. The highest shear stresses and strains were found in this area. At the critical location, the elastic finite element analysis gave:

Maximum shear stress = 6100 psi Maximum shear strain = 0.00855 in/in.

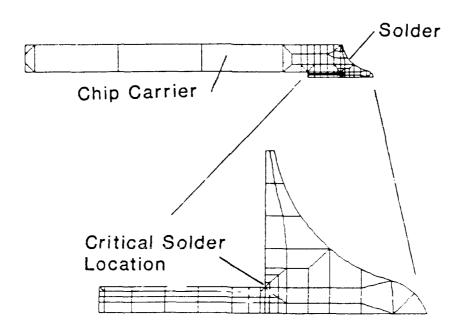


Figure 6-10. 2-D Model of a Leadless Chip Carrier and Solder Joint

The shear stress-strain curve in Figure 6-11 was constructed with data from Reference 6-3 and assuming a proportional limit of 2000 psi. The 6100 psi stress obtained with finite element analysis indicates that plastic deformation occurs in the solder at the critical location.

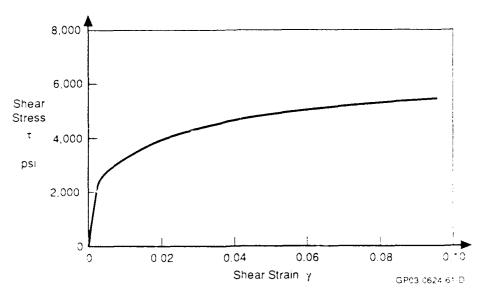


Figure 6-11. Shear Stress-Strain Curve for Solder 63-37

The procedures outlined in Section 4.3.4 were used to determine the actual nonlinear stress and strain state from the linear finite element analysis. The first approximation assumes that the actual shear strain is the same as the calculated strain. The actual stress is then obtained from the shear stress-strain curve in Figure 6-11. This procedure, known as the "linear rule", gives the following actual conditions:

Actual maximum shear stress = 3100 psi Actual maximum shear strain = 0.00855 in/in.

The second procedure used the following "Neuber's rule" calculation:

Elastic FEA stress x strain = 
$$6100 \text{ psi x } 0.00855 \text{ in/in}$$
 Eq. 12  
=  $52.155 \text{ psi in/in}$ 

The actual stress and strain are obtained by finding a point on the stress-strain curve (Figure 6-11) that gives this product. Neuber's rule gives:

Actual maximum shear stress = 3600 psi Actual maximum shear strain = 0.0145 in/in.

The solder experiences these peak stresses when the maximum temperature is reached. These stresses are caused when the PCB expands more than the chip carrier which induces

solder joint deflections. The temperature and deflection is maintained until stress relaxation occurs (Figure 6–12). After power–off, the temperature returns to its original level and the stresses are reversed as the circuit board contracts. Stress relaxation returns the solder to the initial state of stress.

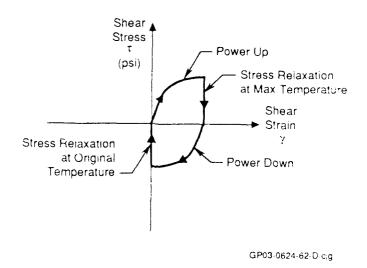


Figure 6-12. Solder Stress-Strain Cycle in a Leadless Solder

Once the stress and strain cycle is defined, the number of cycles to failure can be predicted from available fatigue data. Two alternate procedures are used in this example to predict the life. The first uses the calculated stress to predict life from a plot of stress vs. cycles. The second method is based on effective strain to predict life.

# 6.2.2 Fatigue Life Prediction Based on Stress

The maximum shear stresses estimated from the finite element analysis results were used to predict the number of cycles to failure. The S-N data used is illustrated in Figure 6-5. The following fatigue lives were obtained:

"Linear rule" shear stress = 3100 psi

Predicted Life: 15,000 cycles

"Neuber's rule" shear stress = 3600 psi

Predicted Life: 3000 cycles

The range of fatigue lives obtained with this method is conservative. Although the stresses are fully reversed in Figure 6–12, the strain varies from 0 to a maximum value. The data in the S–N curve in Figure 6–5 corresponds to fully reversed stresses and strains, and therefore, gives shorter lives than expected for this example problem.

# 6.2.3 Fatigue Life Predictions Based on Effective Strain

The effective strain parameter described in Chapter 5 was used to address the effect of non-reversed strains on life. The strain vs. life data in Figure 6–13 (References 6–3 and 6–4) was converted to effective strain vs. life. Data points from Figure 6–13 were selected and converted by using the following relation:

$$\gamma \text{eff} = \sqrt{\frac{\tau_{\text{max}}}{G}} \frac{\Delta \gamma}{2}$$
 Eq. 13

where:

 $G = Shear Modulus = 7.14 \times 10^5 psi$ 

 $\Delta \gamma$  = Shear strain range =  $\gamma_{max} - \gamma_{min}$ 

 $\tau_{\text{max}}$  = Maximum shear stress at the peak of the cycle

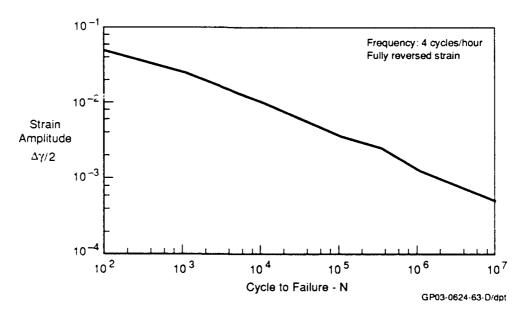


Figure 6-13. Strain-Life Curve for 63-37 Solder at Room Temperature

The following points selected from Figure 6-13 illustrate the conversion:

$\Delta \gamma / 2$	N
0.01	$10^4$
0.025	10 <sup>3</sup>
0.05	10 <sup>2</sup>

The maximum stress of the cycle can be read from the stress-strain curve in Figure 6-11. These values are then used with Equation 13 to compute the following effective strain for each data point:

$\Delta \gamma / 2$	$\tau_{\rm max}$ (psi)	<u>yeff</u>
0.010	3250	0.0067
0.025	4150	0.0121
0.050	4900	0.0135

Values of  $\gamma_{eff}$  and N were then plotted in Figure 6–14

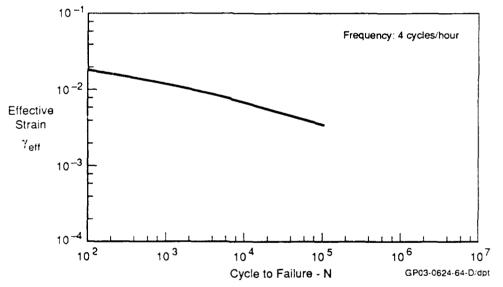


Figure 6-14. Effective Strain vs Life for 63-37 Solder

The next step in the analysis is to determine the effective strain for the thermal cycle used in this example. The "linear rule" approximation resulted in the following values of maximum stress and strain range:

$$\tau_{\mu\alpha\chi}$$
 = 3100  $\pi\sigma$ 1
 $\Delta\gamma$  = 0.00855

Substituting these values into Equation 13 gives:

yeff = 0.0043

From Figure 6-14:

N = 48,000 cycles

Neuber's rule resulted in:

 $\tau_{\text{max}} = 3600 \text{ psi}$ 

 $\Delta \gamma = 0.0145$ 

Substituting into Equation 13 gives:

yeff = 0.00605

and from Figure 6-14:

N = 15,000 cycles

This last value of life represents a reasonable reliability prediction for solder under the 50 degree C thermal cycles.

# 6.3 Dual-Inline-Package (DIP) Lead/Solder Fatigue Analysis

The following is a list of parameters used in the DIP analysis.

Failure Mechanism - Fatigue Cracking

Failure Theory - Stress vs. Cycles to Failure

Device - Inertial Sensor Unit

Component - 40 Pin Dual-Inline-Package

Material - Kovar and Solder

Environment - On-Off Temperature Cycles

This example illustrates non-finite element procedures for analyzing the reliability of lead and solder material connecting a dual-inline-package to a printed circuit board (PCB). The example, extracted from Reference 6-4, is included as an alternate procedure for rapidly assessing electronics life or for checking finite element results.

Consider a 40 pin DIP soldered to a PCB that must operate in an environment where the temperature range is expected to vary from -55°C to 105°C. An examination of the thermal expansion shows that the PCB will expand and contract more than the ceramic DIP component. The expansion differences will force the electrical lead wires to bend as shown in Figure 6-15. A deformation equation can be derived to describe the displacements affecting the lead. The subscripts P and C represent the PCB and the component respectively:

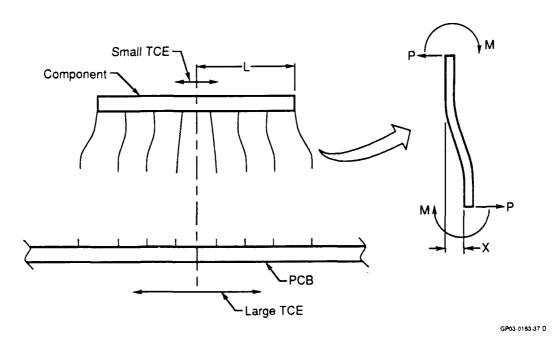


Figure 6-15. Thermal Expansion in Plane

$$X = CTE_p L_p \Delta T - CTE_C L_C \Delta T$$
 Eq. 14

where:  $CTE_P$  = coefficient of thermal expansion of an epoxy fiberglass circuit board = 15 x 10<sup>-6</sup> in/in/C

$$CTE_C$$
 = coefficient of thermal expansion of ceramic DIP body  
=  $6 \times 10^{-6}$  in/in/C

 $L_C$  = length from center to end of DIP

= 1.0 inch

 $L_P$  = effective length of PCB, same as DIP

= 1.0 inch

 $\Delta T$  = temperature amplitude

= [105 - (-55)]/2 = 80°C

X = relative displacement

Note that half the maximum to minimum temperature range is used to find the displacement difference between the PCB and DIP. This assumes that the expansion from the center of the component to one end of the component is the same as the contraction. This also assumes that the cycle duration does not permit stress relaxation and creep in the solder.

Substituting into Equation 14 gives the expansion difference between the PCB and DIP:

$$X = (15 - 6) \times 10^{-6} (1.0)(80)$$
  
= 0.00072 inches Eq. 15

The horizontal force acting on the electrical leads can be determined from the spring rate of the lead and the displacement calculated below. Therefore, the lead spring rate must be obtained in order to obtain the force in the lead. The standard DIP lead has a small horizontal leg that extends outward from the DIP body before it makes a 90 degree bend down, as shown in Figure 6–16. Therefore, when the DIP lead is forced to bend due to the thermal expansion difference, the vertical part of the lead will bend and the

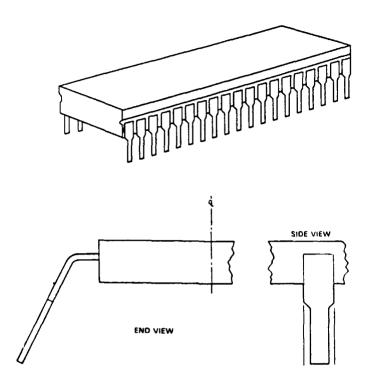


Figure 6-16. Typical DIP Package

horizontal part of the lead will twist, as shown in Figure 6-17. The problem can be simplified by considering only the end lead on the DIP for the bending stiffness. Since the stiffness of the DIP and the PCB along the X axis is much greater than the bending stiffness of all the leads, there will be very little change in the relative displacement when only the end DIP leads are used for the analysis.

Superposition can be used to find the total displacement due to bending and twisting. The lead can be considered as a beam fixed at both ends, with a lateral displacement as follows:

$$X_1 = \frac{P L_1^3}{12 E I_1} = Lead$$
 bending displacement Eq. 16

where:

P = load

E = Young's Modulus

 $I_1$  = Moment of Inertia of lead

 $L_1$  = Lead length, vertical

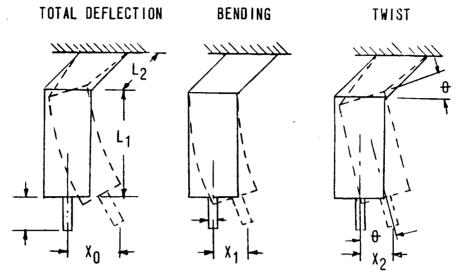


Figure 6-17. DIP Lead Deformation

Considering the torsion in the standard DIP lead next, the horizontal part of the lead will twist through the angle theta  $(\theta)$  resulting in a displacement for this segment of:

$$X_2 = L_1 \theta$$
 Displacement due to wire rotation Eq. 17

The angle of twist, theta, will be related to the torque and the torsional stiffness of the lead as follows:

$$\theta = \frac{T L_2}{G J}$$
 Eq. 18

where:

T = Lead Torque

 $L_2$  = Lead length, horizontal

J = Torsion form factor

G = Shear Modulus

This torque is equal to:

$$T = P L_1$$
 Eq. 19

Substituting Equations 18 and 19 into Equation 17 gives:

$$X_2 = \frac{P L_1^2 L_2}{G J}$$
 Eq. 20

The total lead displacement will be the sum of the two displacements:

$$X = X_1 + X_2$$
 Eq. 21

Substituting Equations 16 and 20 into Equation 21:

$$X = P L_1^2 \left( \frac{L_1}{12 E I_1} + \frac{L_2}{G J} \right)$$
 Eq. 22

The load P on the lead is:

$$P = \frac{X}{L_1^2 \left( \frac{L_1}{12 E I_1} + \frac{L_2}{G J} \right)}$$
 Eq. 23

where:  $L_1$  = Length of vertical wire leg, which includes part of the thinner wire that extends into solder joint in the plated through hole, one wire width of 0.018 inch.

$$= L_{1a} + L_{1b} = 0.156 + 0.018 = 0.174$$
 inch

 $L_2$  = Length of horizontal wire leg = 0.038 inch

d = constant wire thickness = 0.010 inch

h = width at wide part of wire = 0.050 inch

 $h_{1b}$  = width at narrow part of wire = 0.018 inch

$$I_{1a} = d h^3/12 = (0.010) (0.050)^3/12 = 1.042 \times 10^{-7} in.^4$$

$$I_{1b} = (0.010) (0.018)^3 / 12 = 4.86 \times 10^{-9} \text{ in.}^4$$

E = modulus of elasticity for Kovar =  $20 \times 10^6$  psi

J = wire torsion form factor =  $h d^3/3$ =  $(0.050) (0.010)^3/3 = 1.67 \times 10^{-8} in.^4$ 

G = Shear modulus for Kovar =  $8.27 \times 10^6$  psi

A weighted average lead moment of inertia was used to compensate for the sharp reduction in the wire cross section at the narrow segment of the DIP lead.

$$I_{AV} = \frac{L_{la} \ I_{la} + L_{lb} \ I_{lb}}{L_{la} + L_{lb}} \ \text{Average moment of inertia}$$
 Eq. 24

Substituting the various values results in:

$$I_{AV} = \frac{(0.156) (1.042 \times 10^{-7}) + (0.018) (4.89 \times 10^{-9})}{0.156 + 0.018}$$
Eq. 25
$$= 9.39 \times 10^{-8} \text{ in}^4$$

Substituting the above values into Equation 23 results in the load on the lead:

$$P = \frac{0.00072}{(0.174)^2 \left(\frac{0.174}{(12)(20 \times 10^6)(9.39 \times 10^{-8})} + \frac{0.038}{(8.27 \times 10^6)(1.67 \times 10^{-8})}\right)}$$

$$= 0.084 \text{ lb}$$
Eq. 26

The bending moment acting on the lead at the solder joint can be obtained with the following relation:

$$M = \frac{P L_1}{2} = \frac{(0.084) (0.174)}{2}$$
= 0.0073 in - lb

The bending stress at the narrow portion of the lead can be determined from standard bending stress equation:

$$S_b = \frac{M C}{I} = \frac{(0.0073) (0.009)}{4.89 \times 10^{-9}}$$
 Eq.28  
= 13,450 psi

Since the endurance limit for Kovar is about 40,000 psi, the design is safe for the lead material.

The shear tearout stress in the solder joint is considered next. The stress state is caused by forces which pull the lead out of the plated through hole as the board expands. The expression for this relation is:

$$S_{ST} = \frac{M}{h_p A_S}$$
 Solder shear tearout stress Eq. 29

where:

M = Bending Moment = 0.0073 in-lb

 $h_p = PCB$  thickness = 0.080 in.

A<sub>S</sub> = Area of solder section, using an average radii of the solder joint equal to 0.014 in.

$$= \pi (0.014)^2 = 0.000616 \text{ in}^2$$

Substituting results in:

$$S_{ST} = \frac{0.0073}{(0.080) (0.000616)}$$
 Eq.30  
= 148 psi

An examination of the solder fatigue curve in Figure 6–5 shows that the fatigue life for solder will exceed 107 cycles.

# 6.4 Case Study of MMIC GaAs Component for Thermal Reliability

The reliability of a driver amplifier using Microwave/Millimeter-Wave Monolithic Integrated Circuits (MMIC) technology is examined in this example. This component is part of a Transmit/Receive Radar Module as shown in Figure 6-18. The highest heat producing component in the module is the driver amplifier integrated circuit (IC) (Figure 6-19) which produces a peak value of 9 watts of heat and an average value of 2.31 watts. This critical component uses MMIC technology consisting of a gallium arsenide (GaAs) chip and gold metallization with monolithic circuitry containing six field effect transistor (FET) cells. The

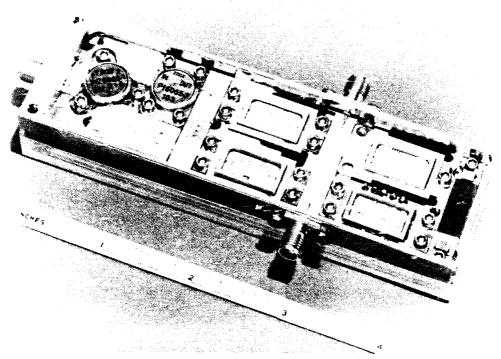


Figure 6-18. Transmit/Receive Module

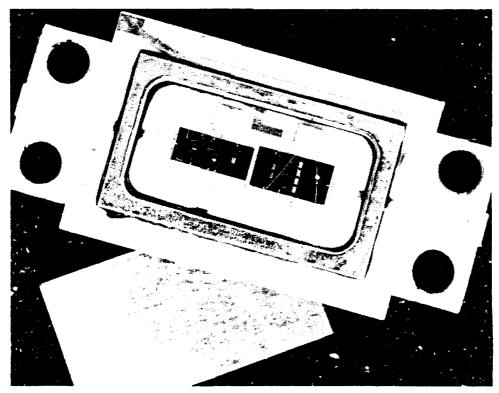


Figure 6-19. Driver Amplifier

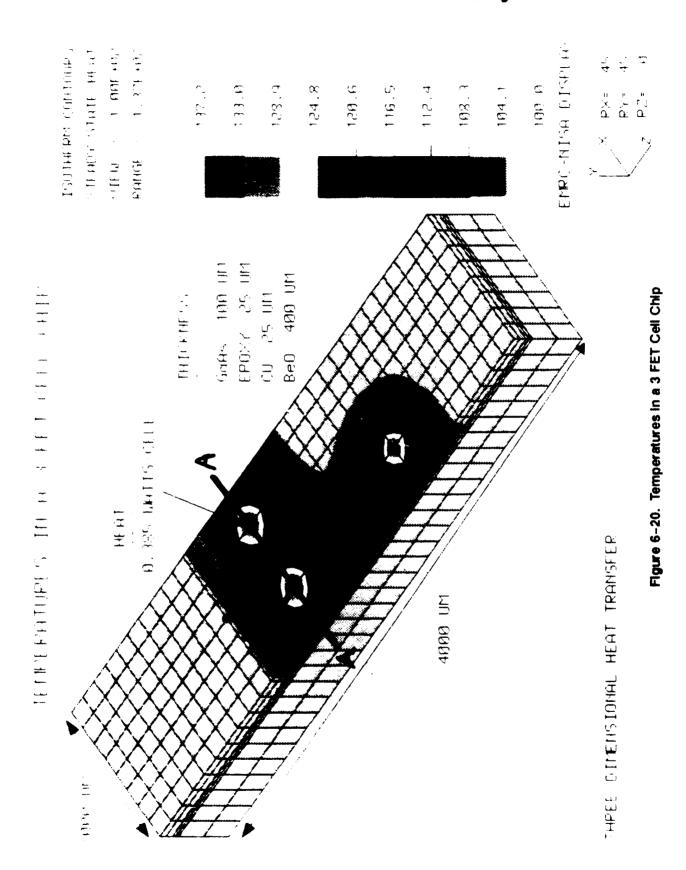
module is attached to a controlled heat sink, and the driver amplifier duty cycle consists of 1 millisecond (msec) on/3 msec off pulses. The pulsing of the amplifier causes temperatures in the component to vary with time. These temperatures vary above and below the average values that would be obtained from steady state, time averaged, heat dissipation thermal simulation. Thus, the stresses vary with time and have a non-zero mean stress. Hence, fatigue data (S-N) must be modified to account for non-zero mean stresses (or R>1).

# 6.4.1 Finite Element Analysis Results

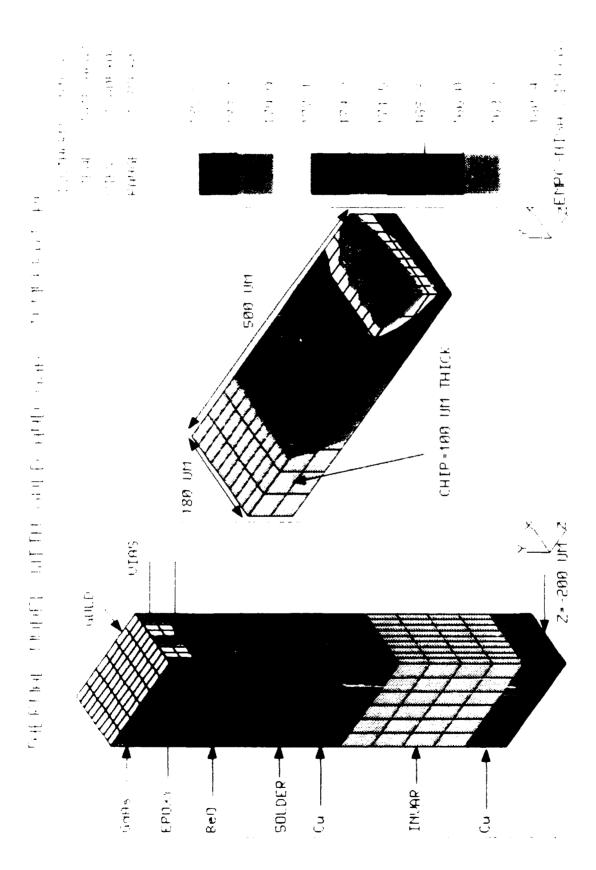
Thermal stress FEA was performed on the component (see Reference 6–5 for further detail on the thermal finite element modeling and analysis). Due to the high concentration of heat being generated in a small area, calculated stresses in some regions of the device are beyond the material's elastic limit. Thus, the linear FEA results were modified to estimate true plastic stresses and strains using Neuber's Rule.

The six FET cells are represented by the FEM shown in Figure 6–20. Only three cells on 1/2 of the chip needed to be modeled because of thermal symmetry along the full chip center line. Also shown are the adiabatic lines of symmetry that define the boundaries of the follow-on 1/4 FET cell model.

The temperature distribution shown in Figure 6–21 is from the thermal transient analysis of the chip and surrounding surface metal at one time step. At this time step, Figure 6–21 represents temperatures at average conditions while Figure 6–22 shows the stresses in the gold metallization at the same instant. Figure 6–23 shows that temperatures vary above and below this condition. Likewise, the stresses will also vary above and below these average values shown in Figure 6–22. For reference, the stresses are in units of newtons per square micrometer (N/µm²). To acquire maximum and minimum thermal stresses, all nodal temperatures at the maximum and minimum temperature times (either 1 or 5 milliseconds and 4 milliseconds respectively, on Figure 6–23) are read into the thermal stress analysis files. The zero stress state is assumed to be at room temperature, 20°C.



6-25



3-0 HEAT TRANSFER 174 FET CELL WITH SOURCE AND DRAIN NEIAL

Figure 6-21. Thermal Model With Gold and GaAs Temperatures

PRINCIPAL STRESSES IN GOLD NETALLIZATION

SI PRINCPL SIRESS UIEW : -3.13F 85

STRESS CONTOURS

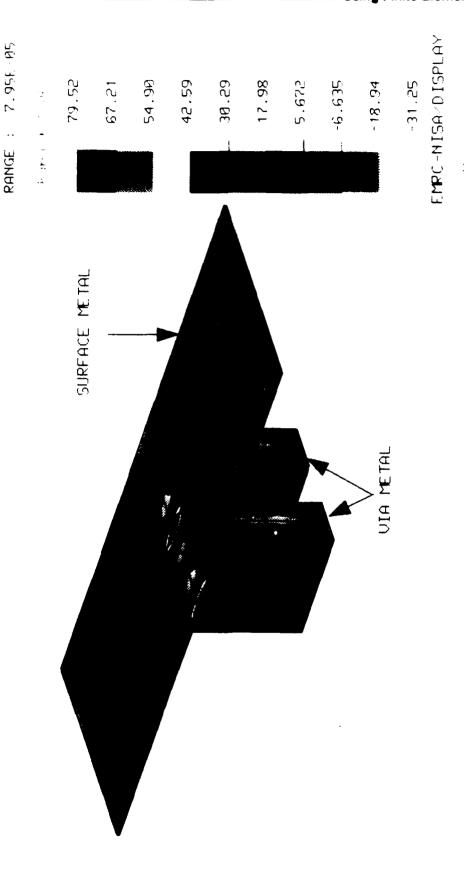
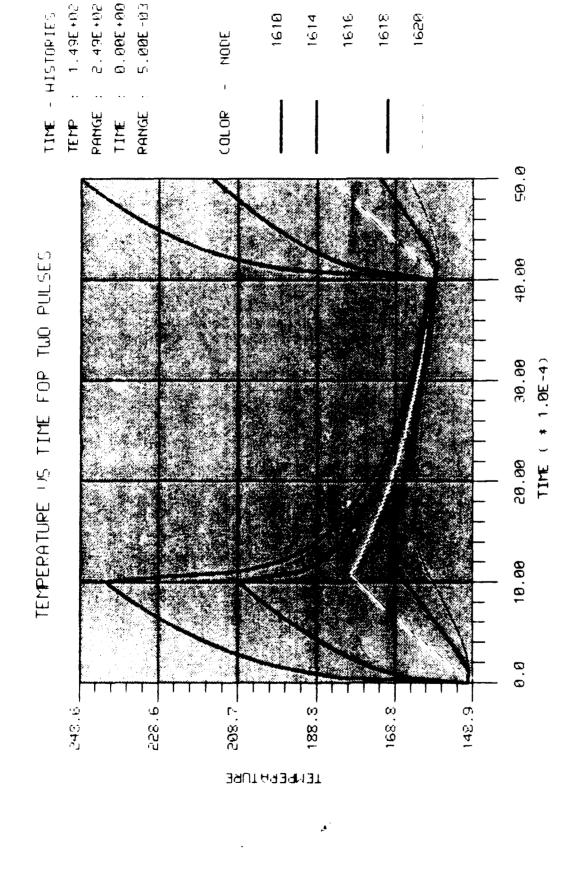


Figure 6-22. Principal Stresses in Gold Metallization

<u>4</u> @

3-D THERMAL STRESS 1/4 FET CELL



/ 1/4 FET CELI

3-E TPANSIENT TRANSFER

Figure 6-23. Temperatures vs Time for Two Pulses

## 6.4.2 Gold Metalization Circuitry Reliability Prediction

The following is a list of the basic parameters and assumptions used in this analysis.

Failure Mechanism - Fatigue Cracking

Failure Theory - Coffin-Manson Plastic Strain vs. Life Analysis

Device - Transmit/Receive Radar Module

Component - Driver Amplifier using MMIC technology

(gallium arsenide chip and gold metallization with

monolithic circuitry containing 6 transistor cells)

Material - Commercial Gold

Environment - Module attached to a controlled heat sink.

Driver amplifier pulsating with a 1 millisecond

on/3 millisecond off pulse

## 6.4.2.1 Linear Stresses and Neuber Rule Approximations

Stress and strain within certain areas of the gold metallization are at stresses that exceed the elastic limit. It is at these locations where the following stresses were acquired using the elastic FEA:

Maximum Tensile Stress – 11,387 psi Average Tensile Stress – 8,540 psi Minimum Tensile Stress – 7,246 psi

Note that for commercial gold, the material's yield point is approximately 1200 psi, and therefore, the gold metallization is undergoing plastic deformations. In order to modify the linear stress and strain to account for plastic deformation, Neuber's relationship is used. Two items are necessary for this calculation: the material's stress-strain curve in Figure 6-24 and the equation:

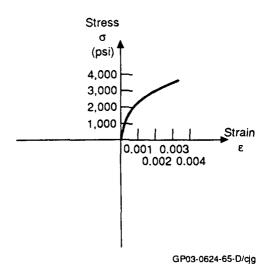


Figure 6-24. Stress-Strain Curve for Gold

$$(\sigma \times \epsilon)_{\text{actual}} = (\sigma \times \epsilon)_{\text{FEA}}$$
 Eq. 31

where:

$$\sigma = stress (psi)$$

$$\epsilon = \text{strain (in/in)}$$

The linear stress and strain are:

$$\sigma_{\text{FEA}} = 11,387 \text{ psi}$$
 $\epsilon_{\text{FEA}} = \sigma/E = 11,387 / 10.8 \times 10^6 = 0.001054$  Eq. 32

where:

E = modulus of elasticity

Finally:

$$(\sigma \times \epsilon)_{\text{FEA}} = (11,387) (0.001054) = 12.0$$
 Eq. 33

The point on the stress-strain curve in Figure 6-24 which gives this product is:

$$\sigma_{\text{actual}} = 3,703 \text{ psi}$$
 $\epsilon_{\text{actual}} = 0.00324$ 

The above values are the stress and strain at maximum temperature:

$$\sigma_{\text{max}} = 3,703 \text{ psi}$$
 $\epsilon_{\text{max}} = 0.00324$ 

A similar procedure can be followed to find the stress and strain at minimum temperature. First the change in the linear stress due to the drop in temperature is computed as follows:

$$\Delta \sigma_{\text{FEA}} = 11,387 - 7,246 = 4,141 \text{ psi}$$
 Eq. 34

The change in strain is given by:

$$\Delta \epsilon_{\text{FEA}} = 4{,}141 / 10.8 \times 10^6 = 0.0003834$$
 Eq. 35

The actual change in stress and strain can be determined by using the hysteresis curve in Figure 6-25 and Neuber's relation one more time. The hysteresis curve was generated by multiplying  $\sigma$  and  $\epsilon$  values of selected data points on the stress-strain curve (Figure 6-24) by a factor of two:

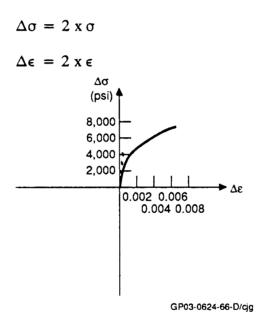


Figure 6-25. Gold Hysteresis Curve

These points were then plotted as  $\Delta \sigma$  vs.  $\Delta \epsilon$ . The hysteresis curve is basically a rescaled stress-strain curve which represents the assumed behavior of the material during unloading. Neuber's rule in this case becomes:

$$(\Delta \sigma \times \Delta \epsilon)_{\text{actual}} = (\Delta \sigma \times \Delta \epsilon)_{\text{FEA}}$$
 Eq. 36

where: 
$$(\Delta \sigma \times \Delta \epsilon)_{FEA} = (4,141) (0.0003834) = 1.588$$
 Eq. 37

The actual  $\Delta \sigma$  and  $\Delta \varepsilon$  values are then read from Figure 6-25 at a point on the hysteresis curve which gives the above product. The actual values are:

$$\Delta \sigma_{\text{actual}} = 2700 \text{ psi}$$
  
 $\Delta \epsilon_{\text{actual}} = 0.00059$ 

The stress and strain at the minimum temperature are:

$$\sigma_{\min} = 3,703 - 2,700 = 1003 \text{ psi}$$
 Eq. 38  
 $\epsilon_{\min} = 0.00324 - 0.00059 = 0.00265$ 

In summary, the stress and strain values at the maximum an minimum temperatures are:

FEA Stress	Actual Stress	Actual Strain
Max 11, 387 psi	3,703 psi	0.00324 in/in
Min 7,246 psi	1,003 psi	0.00265 in/in

# 6.4.2.2 Thermal Cycles to Failure

The Coffin-Manson formula that relates strain to number of cycles to failure will be used. The formula is modified such that only plastic strain will be considered. The strain values acquired from the Neuber analysis include both the elastic and plastic portions. However, the strain value will be assumed to be all plastic. Figure 6-24 shows this simplification to be justified. The Coffin-Manson formula (References 6-6 and 6-7) is:

$$N = \frac{1}{2} \left( \frac{D}{\frac{\Delta \epsilon}{2}} \right)^{1/c}$$
 Eq. 39

where: D = material ductility (in/in)

c = ductility exponent

 $\Delta \epsilon/2$  = strain amplitude

= one half of strain range (in/in)

This formula applies to fully reversed cyclic loading with a zero mean stress. Our loading is not fully reversed (Figure 6-26). In order to account for the change in fatigue life caused by a non-zero mean stress cyclic loading, effective strains,  $\epsilon_{\rm eff}$ , are computed. The number of cycles to failure are then calculated using  $\epsilon_{\rm eff}$  vs. number of cycles to failure data. The effective strain is given by:

$$\epsilon_{\text{eff}} = \sqrt{\frac{\sigma_{\text{max}}}{E}} \frac{\Delta \epsilon}{2}$$
 Eq. 40

where:

 $\epsilon_{\rm eff}$  = the effective strain (in/in)

E = modulus of elasticity = 10.8 x 106 psi

 $\Delta \epsilon = \text{strain range (in/in)}$ 

 $\sigma_{max}$  = the maximum stress in the cycle

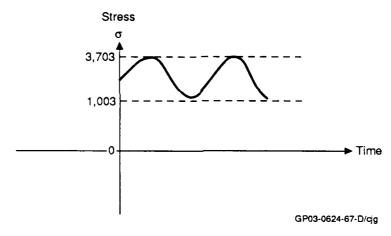


Figure 6-26. Stress History

The temperature excursions experienced by the component results in the following stress and strains in the gold:

$$\sigma_{\mu\alpha\chi} = 3,703 \text{ mg}_1, \ \epsilon_{\mu\alpha\chi} = 0.00324 \text{ iv/iv}$$

$$\sigma_{\mu\nu} = 1,003 \text{ mg}_1, \ \epsilon_{\mu\nu} = 0.00265 \text{ iv/iv}$$

where:

De = 0.00324 - 0.00265 = 0.00059 in/in

Eq. 41

and: De/2 = 0.00059/2 = 0.000295 in/in

Eq. 42

From the above equation:

$$\epsilon_{\text{eff}} = \sqrt{\frac{3703}{10.8\text{E}6}} \times 0.000295 = .00032$$
 Eq. 43

Data relating  $\epsilon_{\rm eff}$  to the number of cycles to failure can be determined with the Coffin-Manson equation. Using a value of ductility = 0.3 and a ductility exponent = 0.5 for commercial gold, a plot of  $\epsilon_{\rm eff}$  vs. Life (N) is determined as follows:

- 1) Using various values of maximum stress, determine plastic strain amplitude ( $\Delta \epsilon/2$ ) from the stress-strain curve (Figure 6-24).
- 2) Calculate the number of cycles to failure (N) using Equation 39.
- 3) Calculate the effective strain ( $\epsilon_{eff}$ ) using Equation 40 where  $\sigma = \text{maximum stress}$  for each  $\Delta \epsilon/2$  and  $E = 10.8 \times 10^6$  psi.

Sample data points for the  $\epsilon_{eff}$  vs. N curve are:

Maximum Stress v (psi)	Strain Amplitude De/2 (in/in)	N (cycles)	e <sub>eff</sub> (in/in)
3,703	0.00324	4,287	0.0011
3,162	0.00212	10,012	0.0008
2,898	0.00168	15,944	0.0007
2,500	0.00120	31,250	0.0005
2,200	0.00080	70,312	0.0004
2,000	0.00066	103,660	0.00035
1,900	0.00058	132,270	0.00032

For this loading,  $\epsilon_{\text{eff}} = 0.00032$ , and N = 132,270 cycles to failure (Figure 6-27).

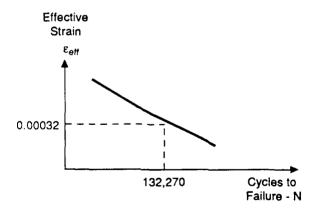


Figure 6-27. Fatigue Life From an Effective Strain vs Life Curve

# 6.4.3 Gallium Arsenide Reliability Prediction

Failure Mechanism - Brittle Fracture

Failure Theory - Maximum Stress Failure Criteria

Device – Transmit/Receive Radar Module

Component - Driver Amplifier using MMIC technology (gallium

arsenide chip and gold metallization with

monolithic circuitry containing 6 transistor cells)

Material - Gallium Arsenide

Environment – Module attached to a controlled heat sink.

Driver amplifier pulsating with a 1 millisecond

on/3 millisecond off pulse

Gallium arsenide is a brittle material with an ultimate strength of 6100 psi. The failure mechanism is brittle fracture, and the component will break if the stresses reach or exceed the strength of the material. The finite element analysis indicates that the thermal stress in the gallium arsenide can reach 12,035 psi. This results in:

$$\sigma_{\text{max}} > \sigma_{\text{ult}}$$
 Eq. 44

where:  $\sigma_{\text{max}} = 12,035 \text{ psi}$  $\sigma_{\text{ult}} = 6,100 \text{ psi}$ 

Therefore, the material is expected to fail at the operational temperatures. These temperatures need to be lowered to bring the thermal stress below the ultimate strength of gallium arsenide.

# 6.5 Lead Buckling Analysis

Failure Mechanism - Buckling

Failure Theory - Euler's Buckling Formula

Device - Flight Control Computer Printed Circuit Board

Component - 68 J-Lead Surface Mounted Chip Carrier

Material - Kovar

Environment – Aircraft Vibration

A finite element analysis simulating a vibration environment is described in Chapter 4. This analysis indicates that some of the leads connecting the surface mount component experience compression while the board vibrates. The load  $(F_{RMS})$  acting on the critical lead was computed with the finite element analysis to be 0.324 lb. During random vibration, peak loads can reach levels four times as high as  $F_{RMS}$ :

Maximum Applied Load, Fapplied = 
$$4 \times F_{RMS}$$
 Eq. 45  
=  $4 \times 0.324 \text{ lb}$   
=  $1.296 \text{ lb}$ 

The critical buckling load is given by:

$$F_{cr} = \frac{4\pi^2 E I}{L^2}$$
 Eq. 46

where:

 $E = modulus of elasticity = 20 x 10^6 psi$ 

L = length of lead = 0.1 inch

I = moment of inertia of lead cross section

= 1/12 (width) (thickness)<sup>3</sup>

 $= 1/12 (0.012) (0.008)^3$ 

 $= 5.12 \times 10^{-10}$ 

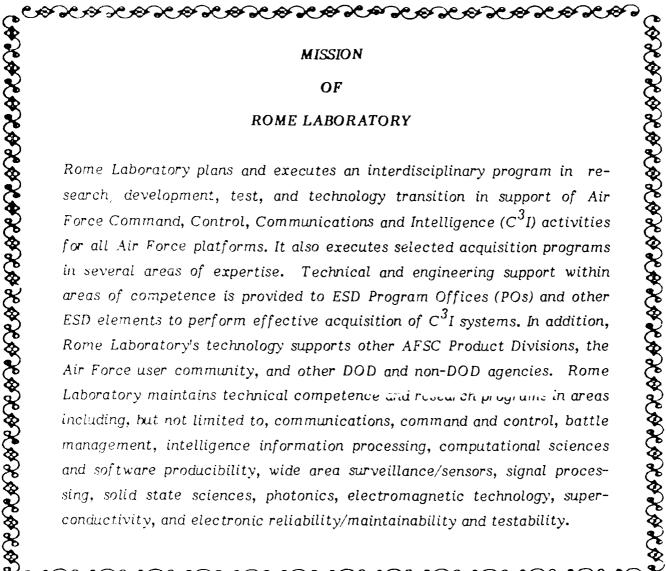
Substituting into Equation (46):

$$F_{cr} = \frac{4\pi^2 (20 \times 10^6) (5.12 \times 10^{-10})}{(0.1)^2}$$
 Eq. 47  
= 40.4 lbs

Because the applied load (1.296 lb) is much smaller than the critical load (40.4 lbs), the lead will not buckle.

#### References

- [6-1] Soovere, J., Dandawate, B.V., Garfinkel, G.A., Isikbay, N., Steinberg, D.S., "Vibration Reliability Life Model for Avionics," AFWAL-TR-87-3048, September 1987.
- [6-2] Engelmaier, W., "Surface Mount Attachment Fatigue Reliability: Accelerated Testing and Predictive Modeling," Presented at the Ninth Annual IEEE/AESS Dayton Chapter Symposium, Dayton, OH, 30 November 1988.
- [6-3] Bae, K., Sprecher, A.F., Conrad, H., Jung, D.Y., "Fatigue of 63Sn-37Pb Solder Used in Electronic Packaging," ISTFA 1988.
- [6-4] Steinberg, D., "Computer Aided Assessment of Reliability Using Finite Element Methods," Subcontractor Report.
- [6-5] Bocchi, W.J., "Thermal Technique Tests GaAs," Mechanical Engineering, August 1990.
- [6-6] Tavernelli, J.F., and Coffin, Jr., L.F., "Experimental Support for Generalized Equation Predicting Low Cycle Fatigue," Trans. ASME, J. Basic Eng., Vol. 84, No. 4, Dec. 1962, p.533.
- [6-7] Manson, S.S., discussion of reference 6.5, Trans. ASME, J. Basic Eng., Vol. 84, No. 4, Dec. 1962, p.537.



### MISSION

## **OF**

### ROME LABORATORY

Rome Laboratory plans and executes an interdisciplinary program in research, development, test, and technology transition in support of Air Force Command, Control, Communications and Intelligence ( $C^3I$ ) activities for all Air Force platforms. It also executes selected acquisition programs in several areas of expertise. Technical and engineering support within areas of competence is provided to ESD Program Offices (POs) and other ESD elements to perform effective acquisition of  $C^3I$  systems. In addition, Rome Laboratory's technology supports other AFSC Product Divisions, the Air Force user community, and other DOD and non-DOD agencies. Rome Laboratory maintains technical competence and research programs in areas including, but not limited to, communications, command and control, battle management, intelligence information processing, computational sciences and software producibility, wide area surveillance/sensors, signal processing, solid state sciences, photonics, electromagnetic technology, superconductivity, and electronic reliability/maintainability and testability.